High Speed ADC Testing

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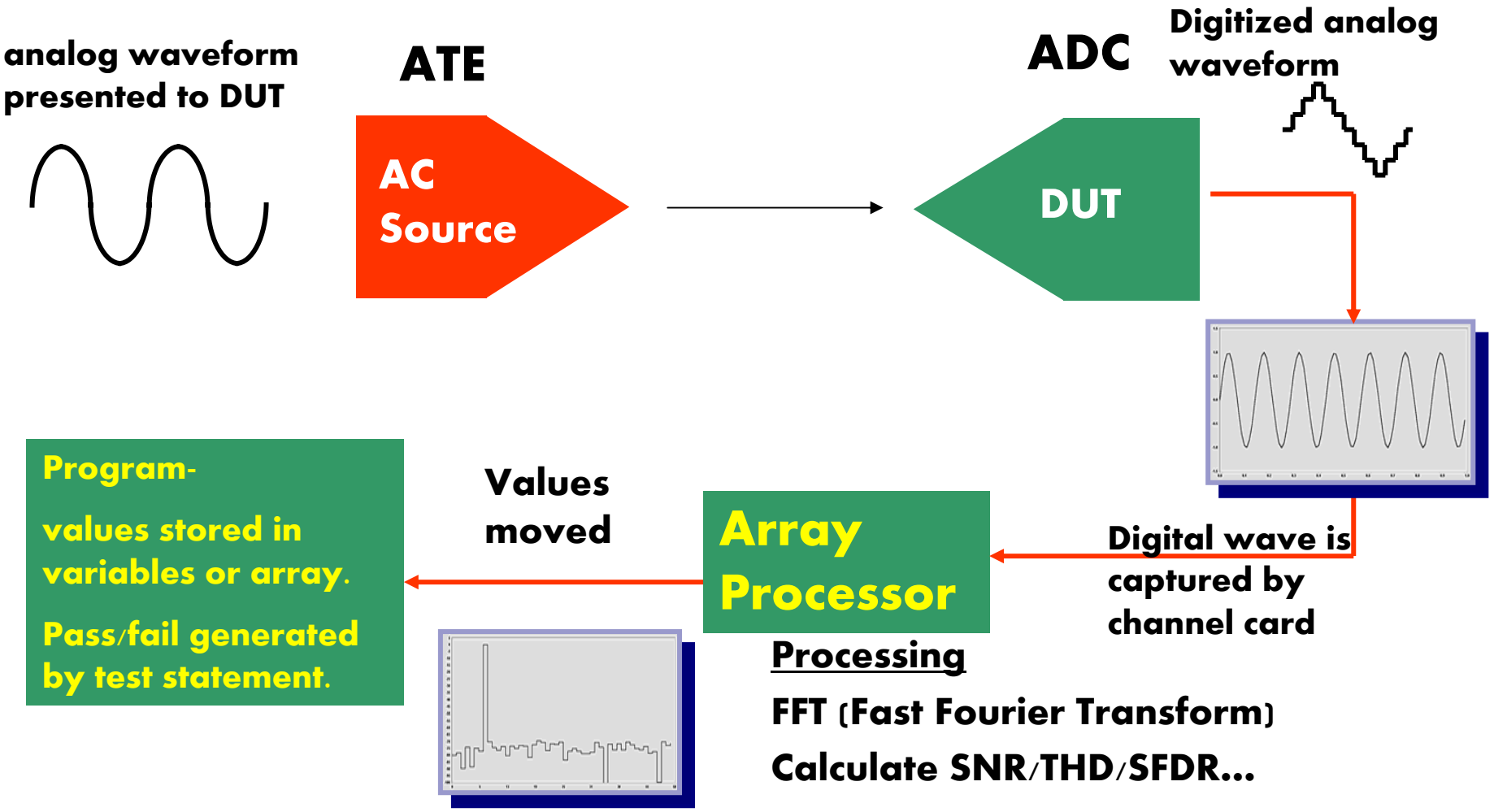
Outline

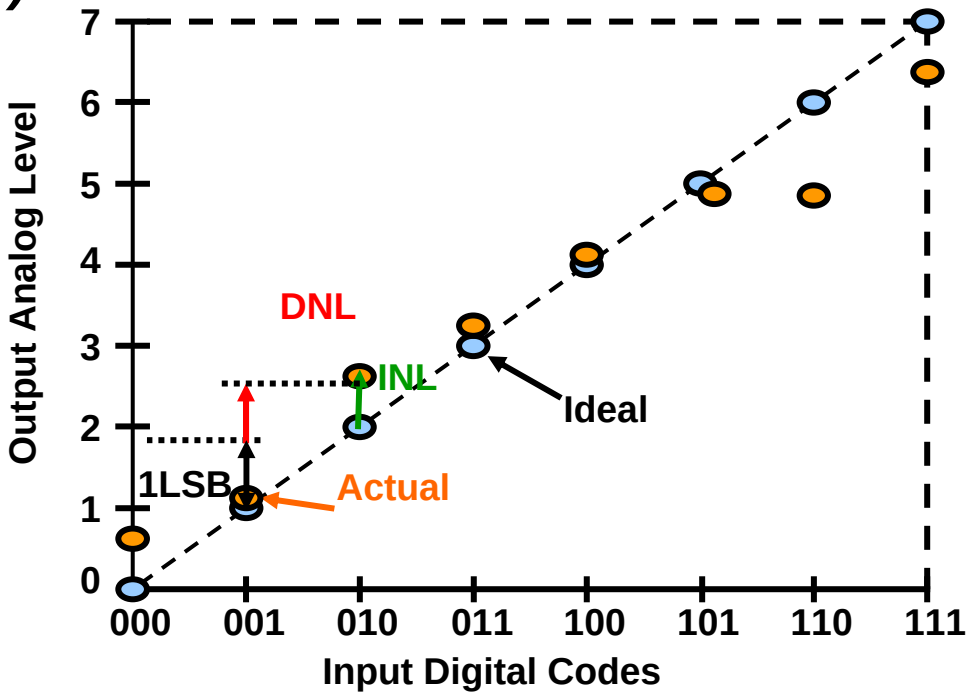
- Mixed-Signal Testing Overview
- Test List / Key parameter
- Limit The Analog Bandwidth
- Flexibility of Terminations
- Resolution VS ENOB
- Clock Jitter effect on ENOB
- Environmental Influences
- Example of High Speed ADC

Mixed-Signal Testing



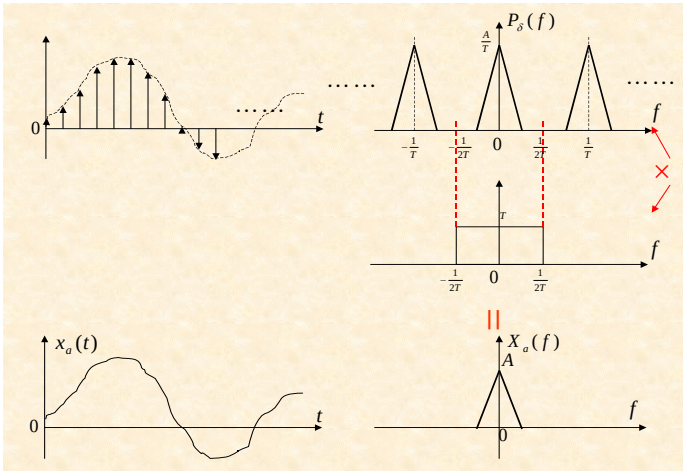
High Speed ADC Test List

- Leakages
- Functional
- Linearity (INL/DNL)
- **SNR**
- THD
- **SFDR**
- Offset/Gain Error
- **ENOB**



Key Parameters

- SNR/SFDR
- Linearity (INL/DNL)



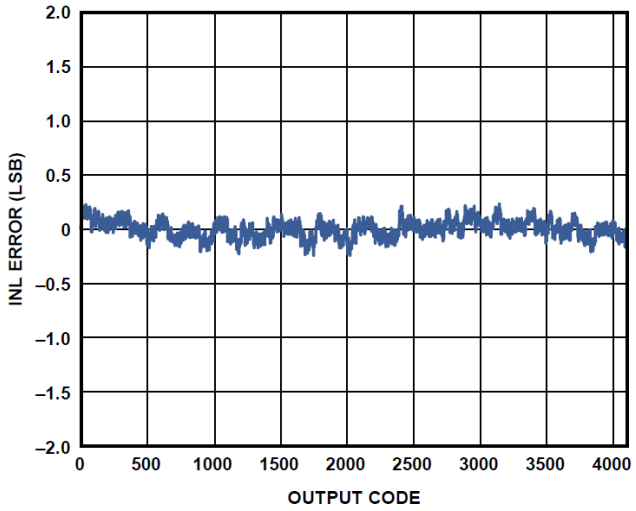


Figure 33. INL Error with f_{IN} = 9.7 MHz

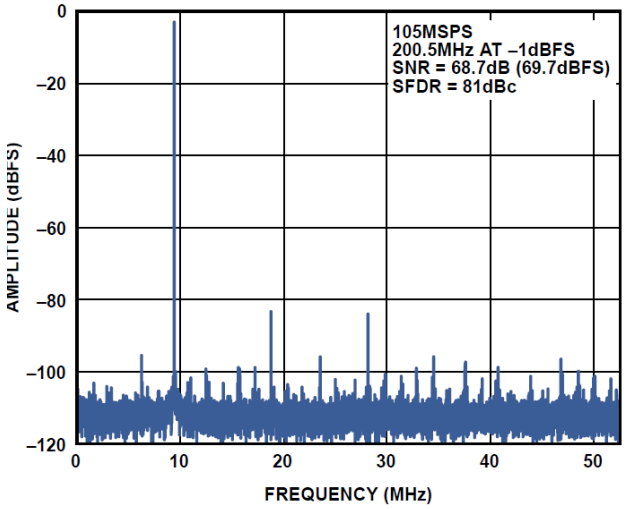


Figure 27. Single-Tone FFT with f_{IN} = 200.5 MHz

Note : From ADI website
http://www.analog.com

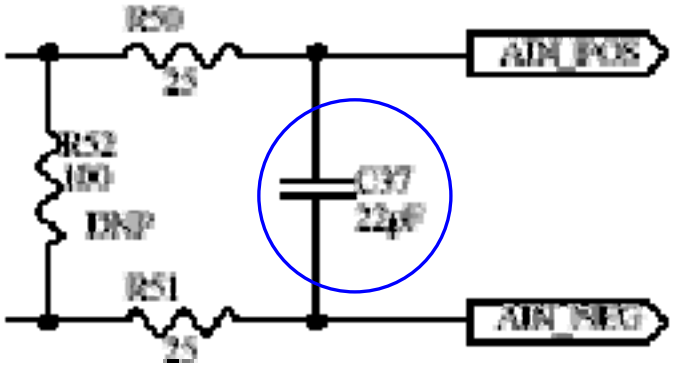
High Speed Converter test

- Choosing the right AC instrument is not the entire solution for high speed converter test
- Proper DIB design and understanding of high performance converter applications is fundamental to achieving performance goals

Limit The Analog Bandwidth

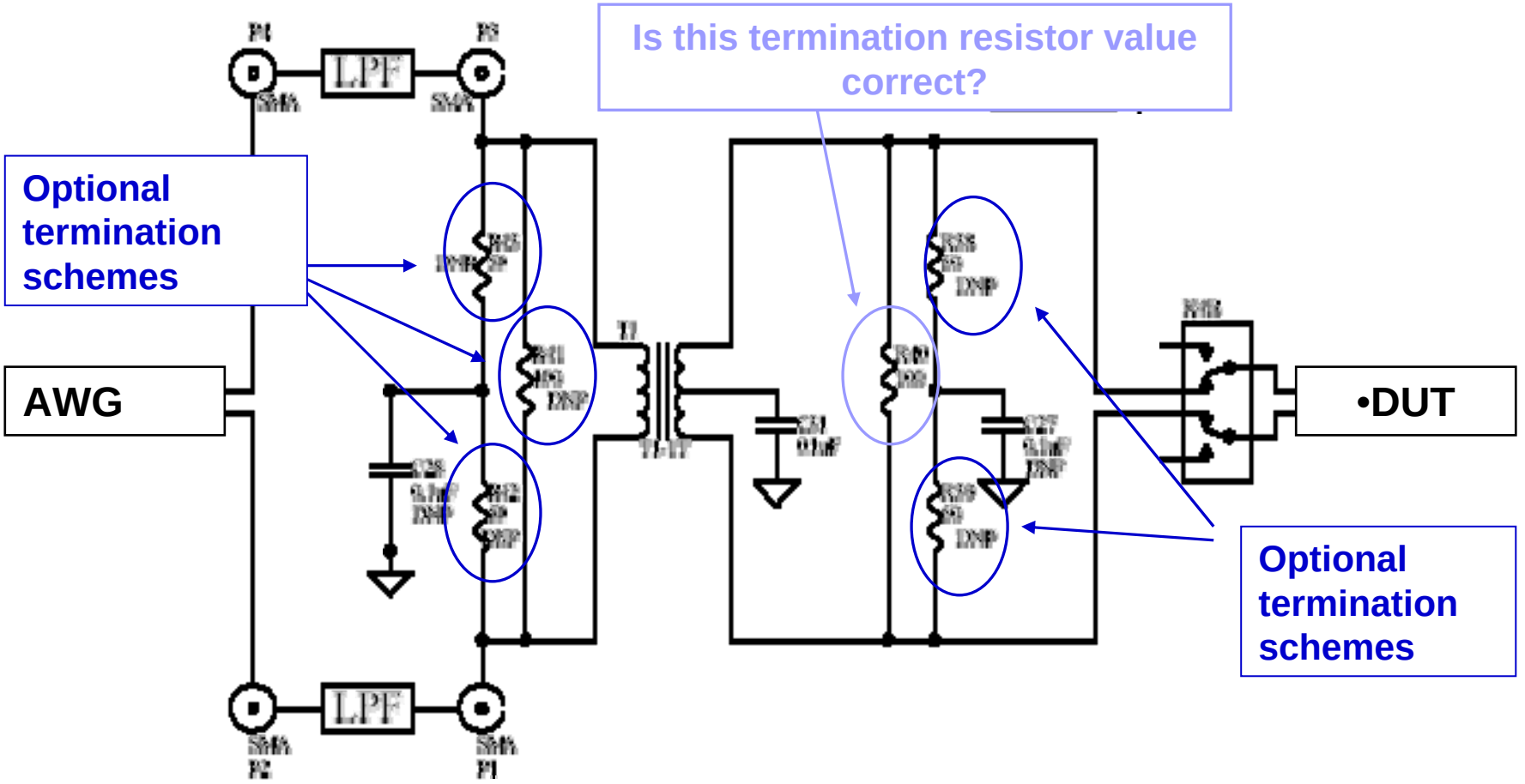
The ADC bandwidth of measurement is not limited to Nyquist!

- **ADC input bandwidth is 550Mhz whereas Nyquist band is 50MHz for 100MHz sample rate.**
- **All noise and spurious from 50MHz to 550MHz will alias into the captured data power spectrum**
- **Use simple first order filter at Nyquist frequency at ADC input pins**
- **Use multiple order bandpass filters to suppress noise and spurs from AC signal source and environment**



The ATE test environment is not perfect. System clocks and external environmental factors will cause spectral impurities in the test signal.

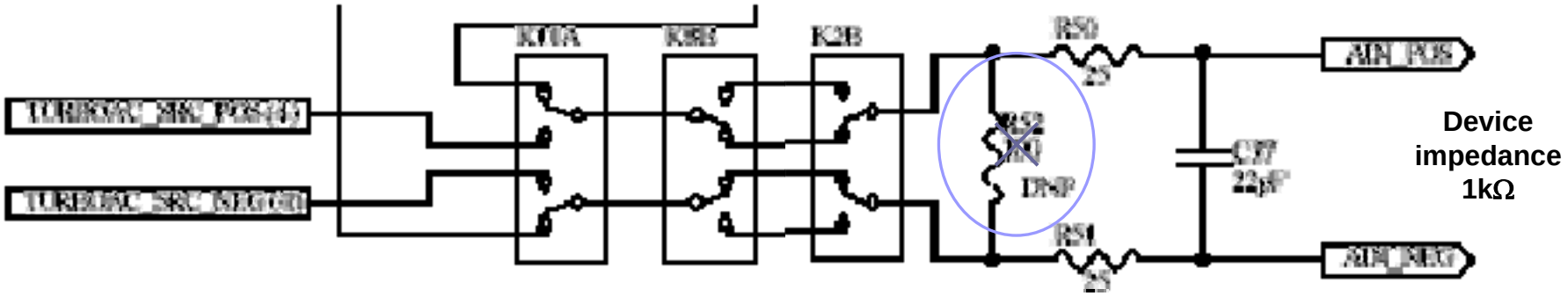
Flexibility of Terminations



Flexibility of Terminations

ADC AC Input Path

AWG mode can drive 100 ohms (diff)



Be Careful !

100 ohms termination resistor here would be 130 ohms total load.

(100+25+25) || (1k device)

Use 61.1 ohms instead to get 100 ohms loading

Resolution VS ENOB

- Resolution ≠ ENOB!
  - Performance of high resolution device maybe worse than low resolution device
- Effective Number of Bits (ENOB)
  - ENOB = (SNRdB – 1.76)/6.02

LTC2389-16 - 16-Bit, 2.5Msps SAR ADC with Pin-Configurable Analog Input Range and 96dB SNR

Features

- 2.5Msps Throughput Rate
- ±1LSB INL (Max)
- Guaranteed 16-Bit, No Missing Codes
- Pin-Configurable Analog Input Range:
  ±4.096V Fully Differential
  0V to 4.096V Pseudo-Differential Unipolar
  ±2.048V Pseudo-Differential Bipolar
- 96.0dB (Fully Differential)/93.5dB (Pseudo Differential) SNR (Typ) at f_{IN} = 2kHz
- –116dB (Fully Differential)/–112dB (Pseudo Differential) THD (Typ) at f_{IN} = 2kHz

VS

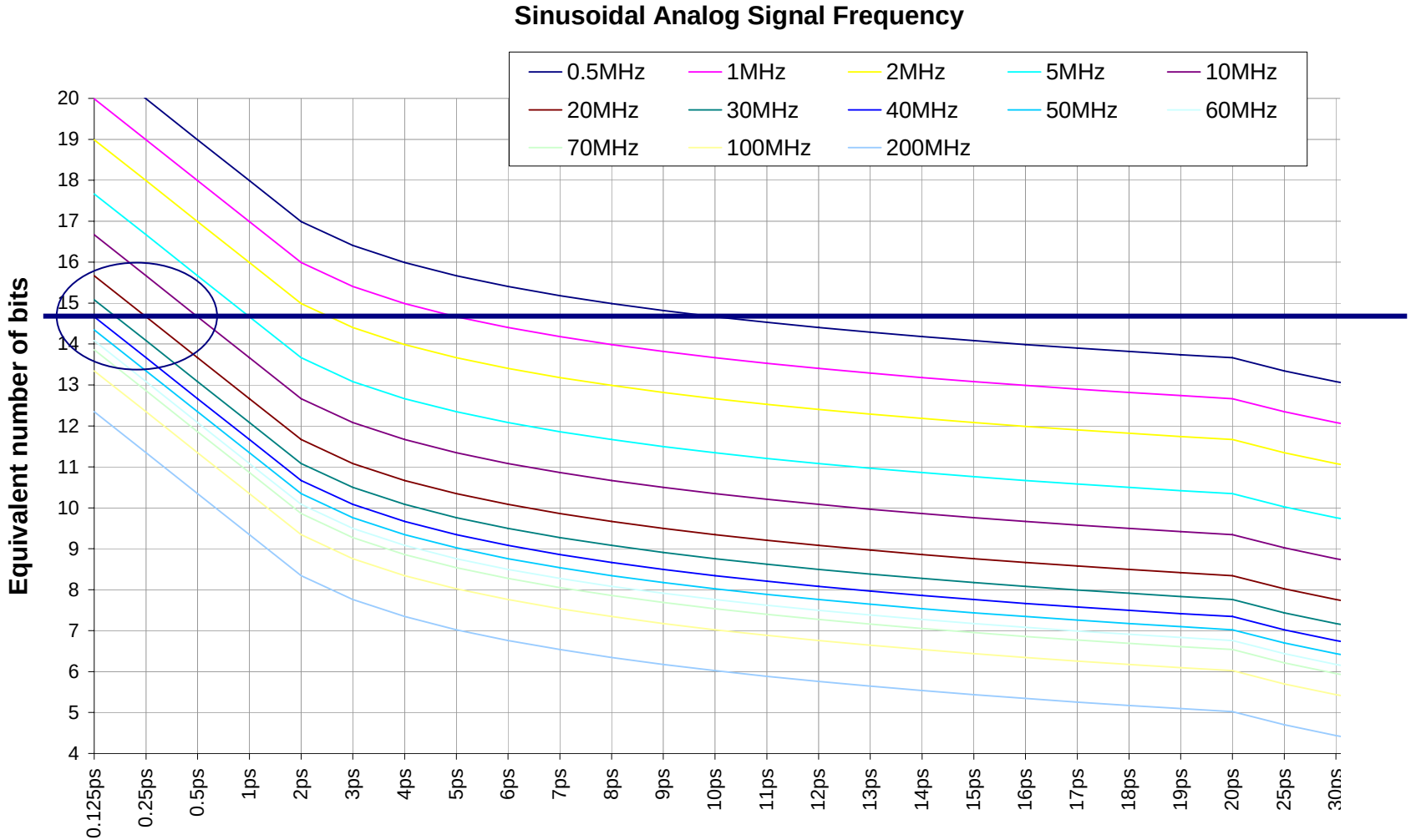
LTC2321-16 - Dual, 16-Bit, 2Msps Differential Input ADC with Wide Input Common Mode Range

Features

- 2Msps Throughput Rate
- ±4LSB INL (Typ)
- Guaranteed 16-Bit, No Missing Codes
- $8V_{P-P}$ Differential Inputs with Wide Input Common Mode Range
- 81dB SNR (Typ) at f_{IN} = 500kHz
- –90dB THD (Typ) at f_{IN} = 500kHz

Note : From Linear Technology
http://www.linear.com/

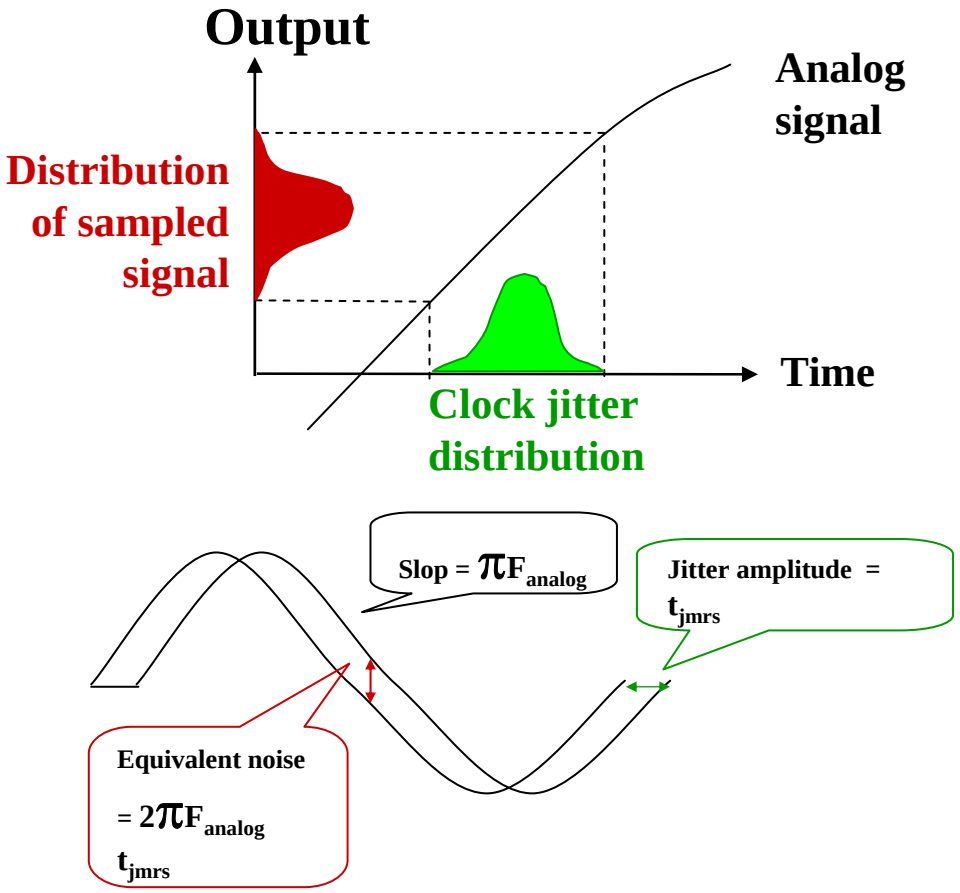
Clock Jitter Effect on ENOB

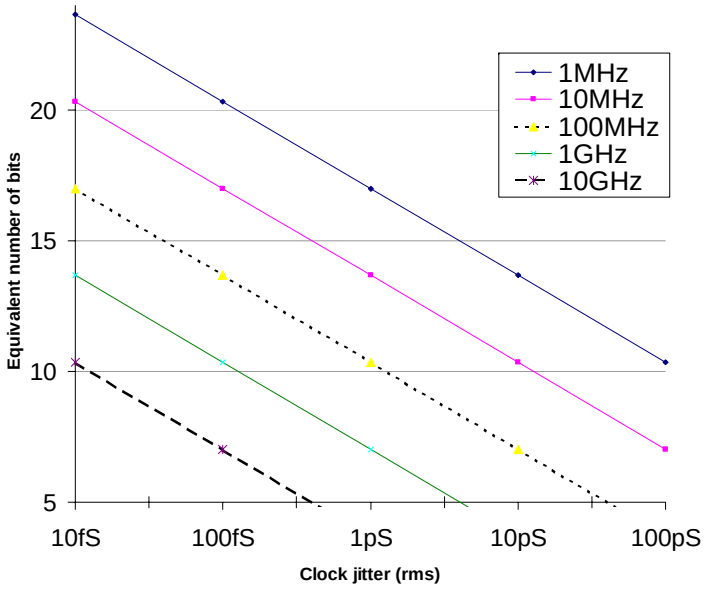


Fi above 10MHz requires <1ps RMS clock jitter for 16-bit converters

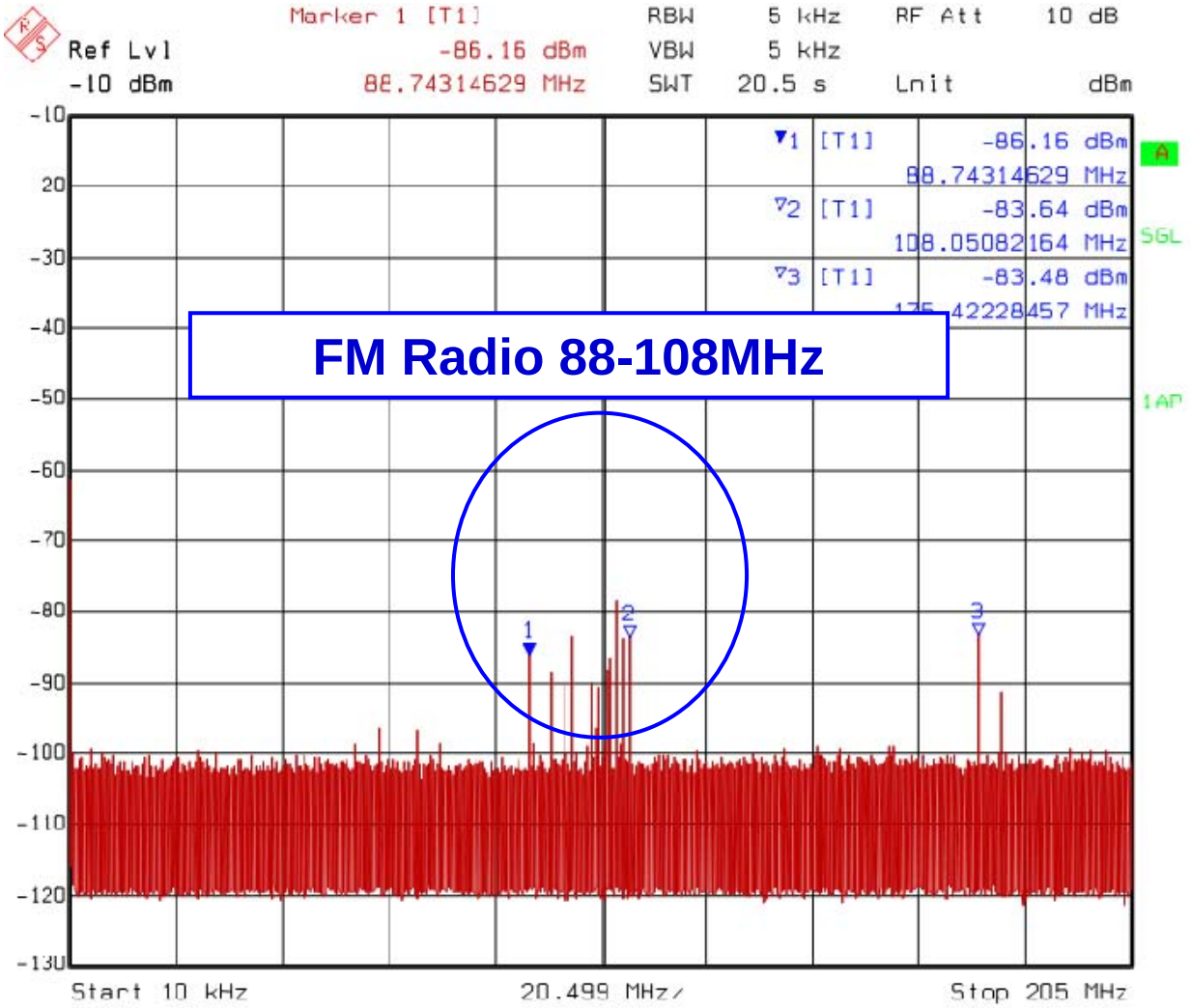
$$SNR = -20 \times \log(2 \times \pi \times fi \times T_j)$$

Jitter Effect in Time Domain



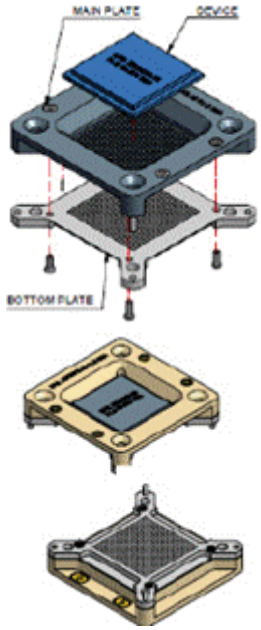


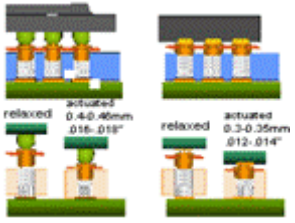
Environmental Influences

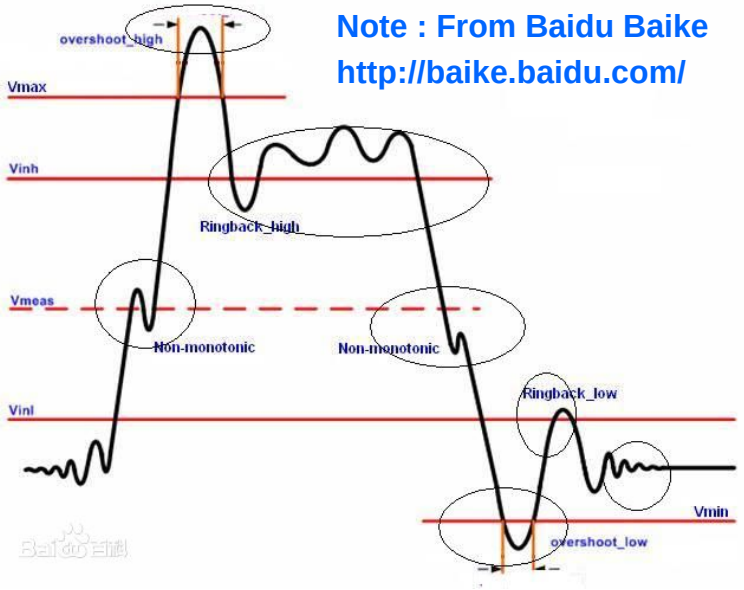


Signal Integrate

- >500Mhz BW for LVDS
- >2Ghz BW for Serial Bus
- Simulation with Socket





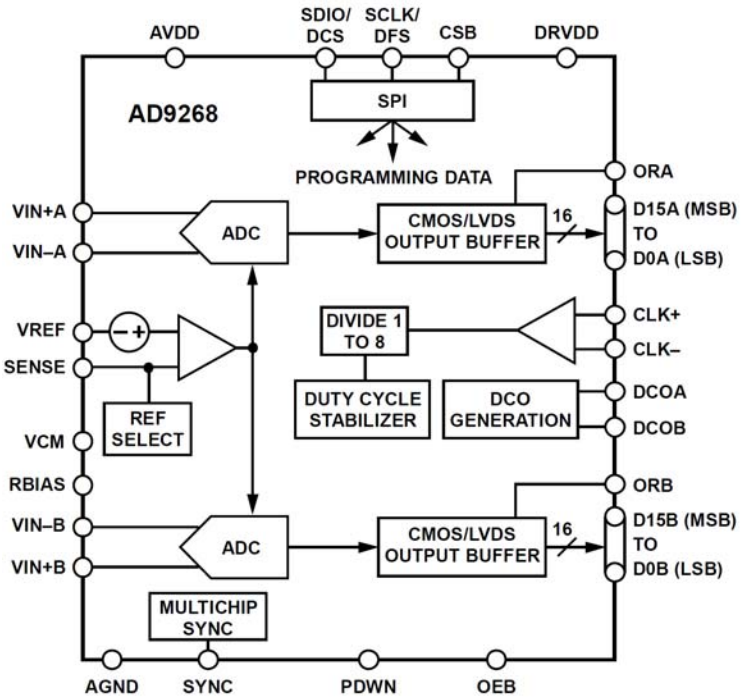


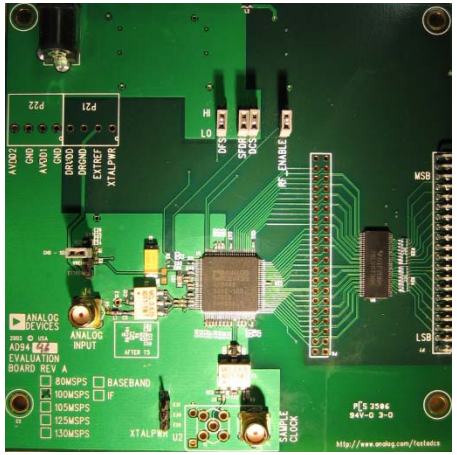
Note : From Baidu Baike
http://baike.baidu.com/

Example of High Speed ADC

AD9628 specifications :

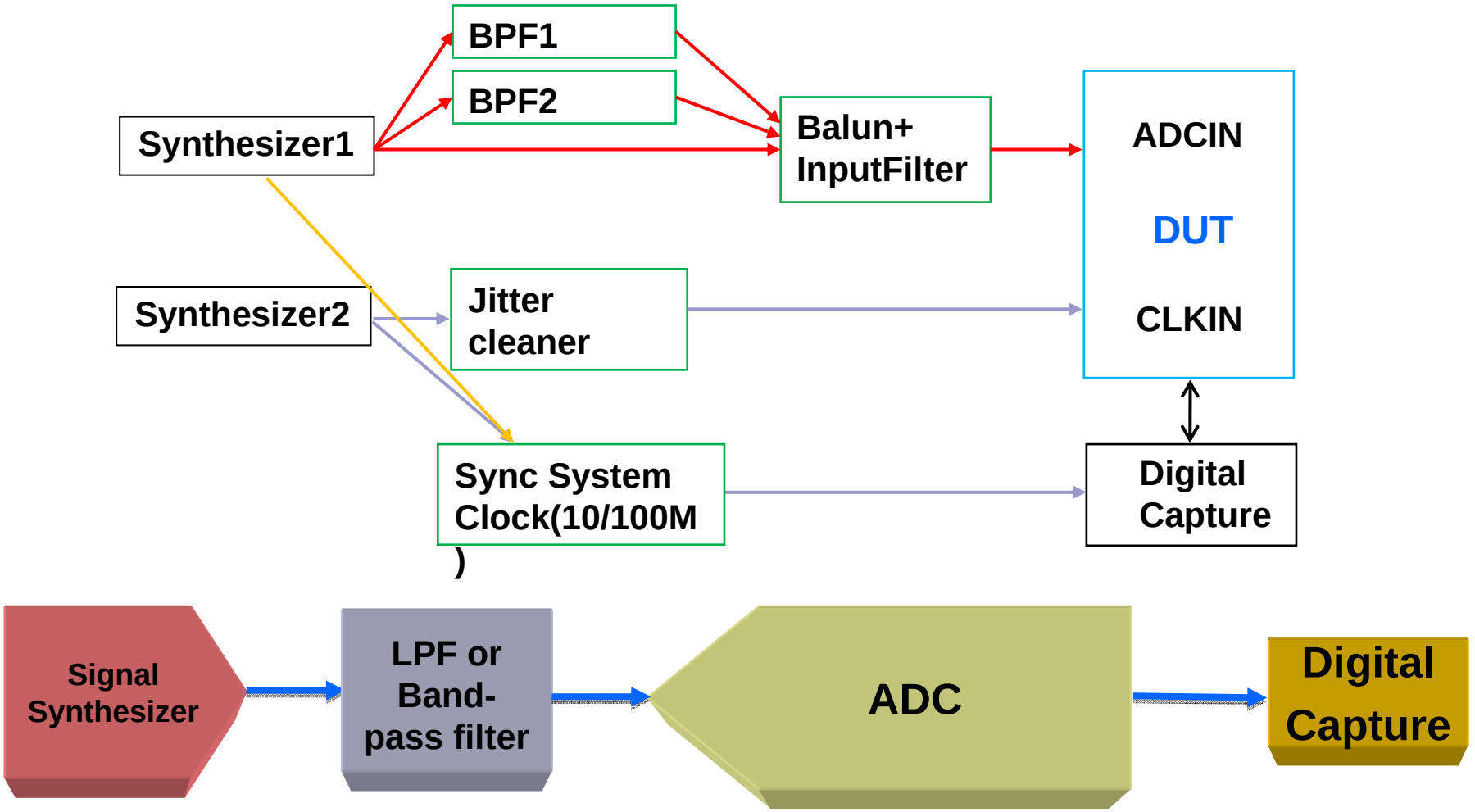
16bits LVDS/CMOS output.
Fs=125Msps.
Input Frequency < 300MHz.
SNR=71.2dBFS @70MHz/125MSPS.
Input Range=2Vpp differential.
Dual channel.
250Msps interleaved outputs.





Note : From ADI website
http://www.analog.com

System Overall

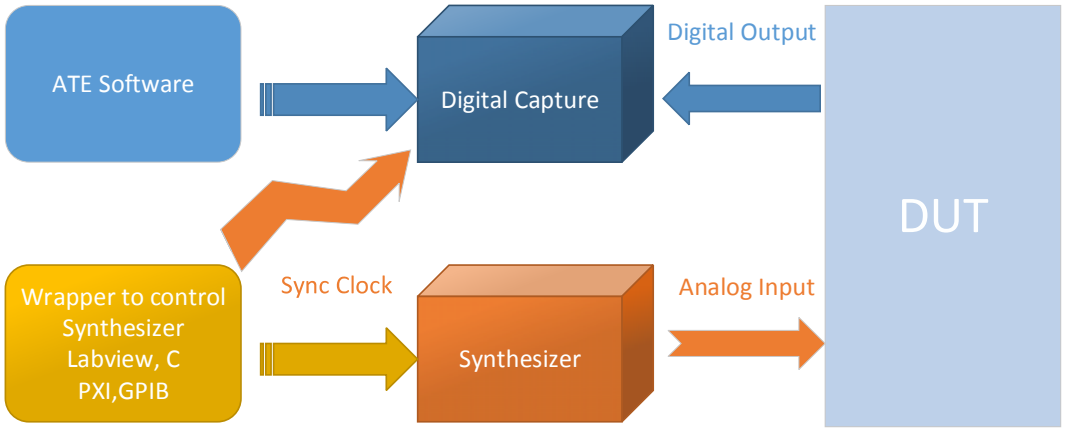


External Synthesizer Driving

Select low phase noise and low wideband noise synthesizer to drive clean clock and waveform

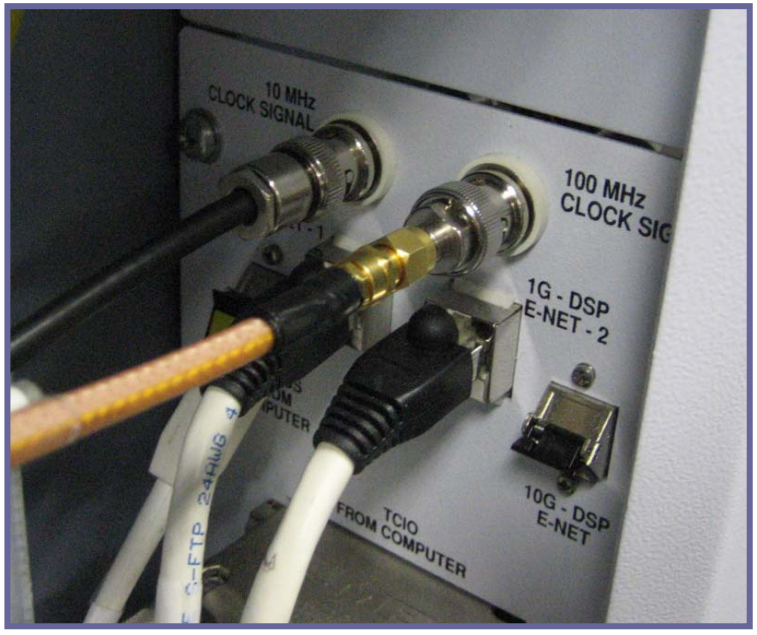
Most Synthesizer units have large amounts of harmonic distortion. Filters must be used with synthesizers.

NI QuickSyn Synthesizer



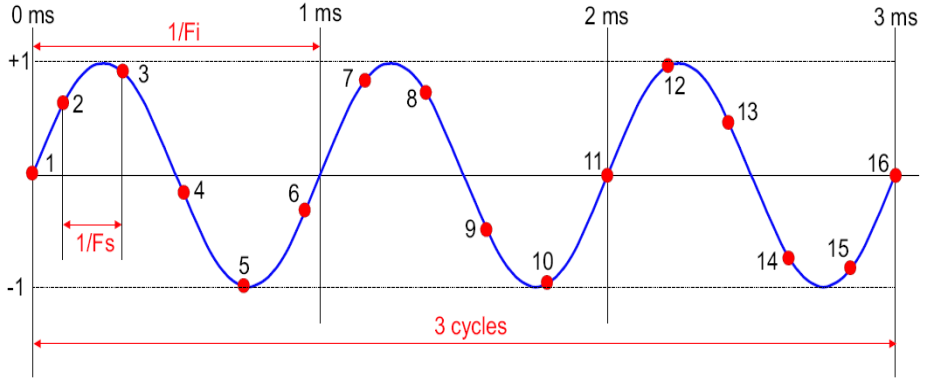
External Synthesizer Driving

Sync all instrument such as ATE, Synthesizer, clock source, Jitter cleaner and so on



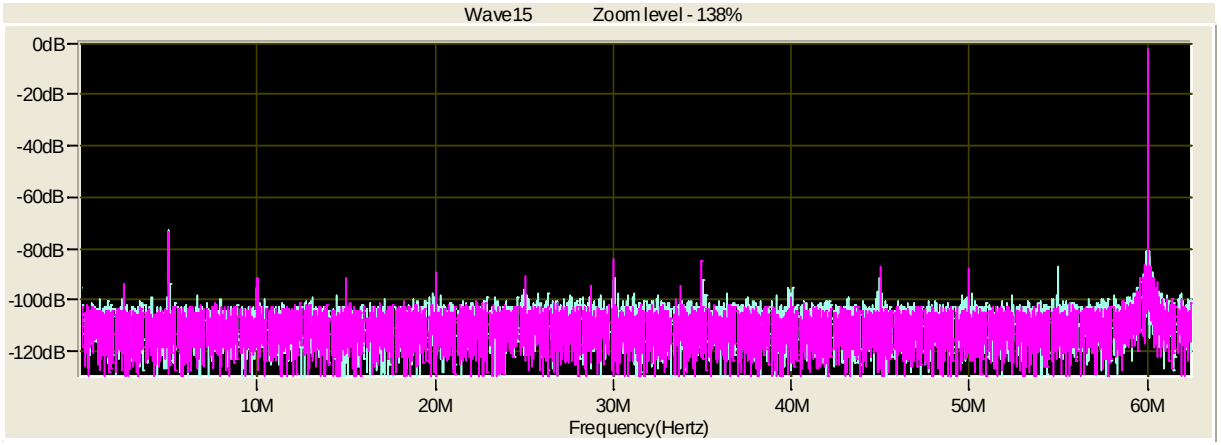
100MHz system reference access panel

For Coherent Sampling



Key Measurements

- Noise, Distortion, Spurious Free dynamic range with each of the following test setup which provides best performance
- ATE AWG as analog source for low frequency measurements (INL/DNL, <10MHz)
- low-noise synthesizer for high frequency
- Low Jitter clocking, 100MHz system reference or synthesizer
- Low pass or Band-pass filtering on DIB



Fs=125MHz
Ft=200MHz
N=16384

Thanks

Q&A