

TERADYNE

## Introducing the Teradyne **FLEX** Test System

and its differences to J750



Because technology never stops

# Introducing the *FLEX*



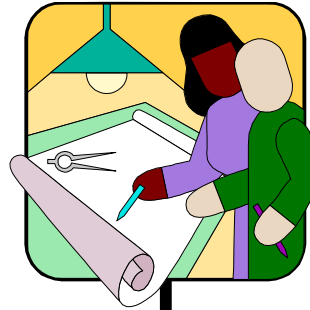
# Integrating Teradyne's Strengths



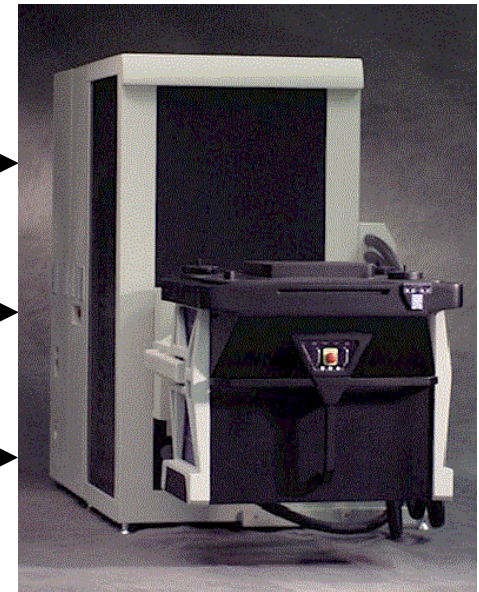
- Analog instrumentation performance/breadth
- 3 generations of mixed-signal test architectures



- Low cost, CMOS-based design
- IG-XL software ease-of-use
- High instrument density

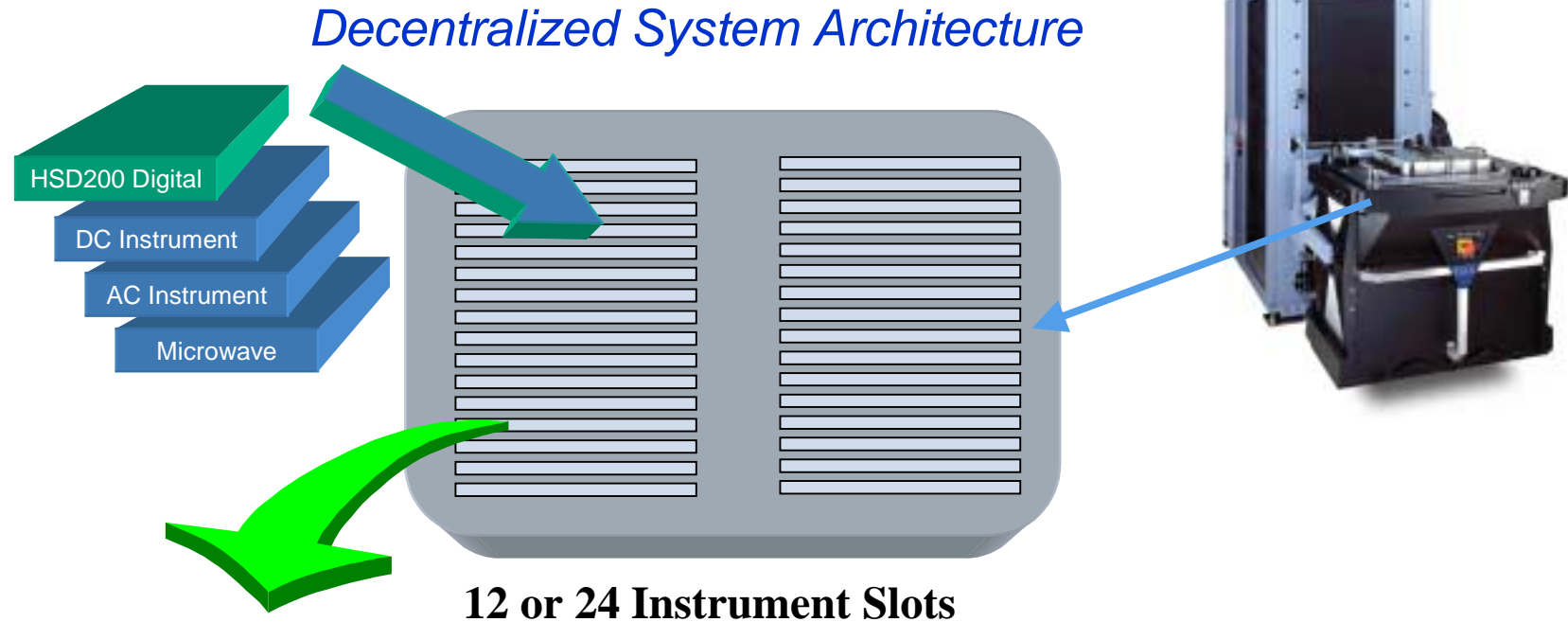


- Breakthrough R&D
- Applications expertise



- **Breakthrough in mixed-signal SOC economics**
- IG-XL software for ease-of-use, compatibility
- Analog instrumentation breadth and performance
- 4th generation mixed-signal architecture

# Universal Slot Test Head



## Universal Slot Test Head – *Scalable Performance*

**Air Cooled** slots for optimal economics

**Cable Connect DIB** for flexible configuration of signal delivery

**Direct Access** to the Sync-Link and Background DSP Architecture

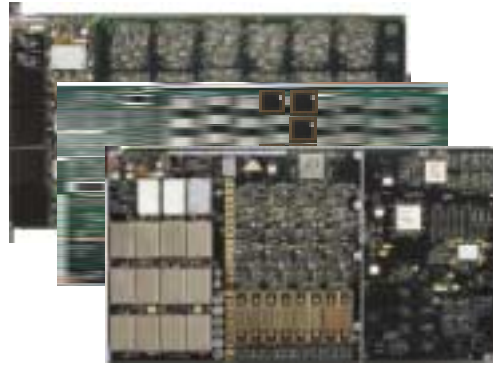
**IG-XL Vertical Sliced Instrument Software**

# FLEX is highly configurable

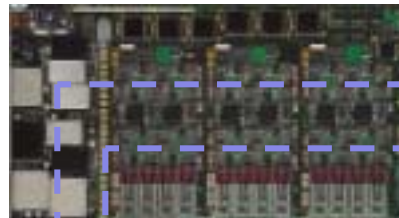
Universal slot test head



High density single board instruments



- 48 ch 200 MHz digital
- 24 ch 25 V digital, 75 V PMU
- 8 ch octal op amp loop
- 20 ch 30 V / 200 mA dynamic DC
- 6 ch 15 A dynamic DC
- 4 ch 75 V / 2 A dynamic DC
- 4 ch 90 V dynamic DC
- 4 ch 15 MHz, source and capture
- 4 ch VHF AC source & capture
- 2 ch Low jitter 1 GHz clock
- 11 ch 6G Microwave



- Future capability
- High density device power supply
  - High density digital
  - Open Architecture designed instruments

**High density instruments and universal slot test head key to field reconfigurability**



**64 Channels per Board**

**100 MHz**

**512/1024 I/O Pins**

**4 / 16 Meg Per Pin Vector  
Memory with integrated Scan**

**Flexible Pattern and Timing  
Architecture**

**x32 True Parallel Test**

**Full suite of instruments:**

⇒ ***SCAN***

⇒ ***Converter Test Option***

⇒ ***Memory Test Option***

⇒ ***High Voltage Drivers***

⇒ ***Mixed Signal Option***

# J750 and FLEX Instrumentation comparison

## J750

### □ Digital

- 64 channels digital
- Maximum 16 slots (max. 1024 channels)
- Build-in option
  - digital signal source/capture (DSIO)
  - memory test option (MTO)
  - scan option

### □ DC and Power

- DPS - 8 ch 1A VI
- APMU - 64 ch 35V HV digital

### □ Mixed Signals Instrument

- Mixed Signal Options (MSO)
- Converter Test Options (CTO)

## FLEX

### □ Digital

- 48 channels digital
- Maximum 24 slots (max. 1152 channels)
- Build-in option
  - digital signal source/capture (DSSC)
  - memory test option (MTO)
  - scan option

### □ DC and Power

- DC30 - 20 ch 30V/200mA VI, TMS/meter
- DC75 - 4 ch 75V/2A VI, TMS/meter
- DC90 - 4 ch 90V/10A pulsed VI, TMS/meter
- HVD - 24 ch 25V HV digital, 75V PPMU
- HexVS - 6 ch 6V/15A, merge to 90A

### □ Mixed Signals Instrument

- Baseband (BBAC)
- Very High Frequency (VHFAC)
- Microwave RF instrument

## J750

### • Digital channel

- **Channels per board** – 64 channels
- **Maximum Large vector memory** – 16 Meg
- **Maximum board per tester** – 8 /16
- **Maximum channels per tester** – 512/1024
- **Maximum vector rate** – 100Mhz
  
- **Pin Level**
  - **vil range** - -1 to + 6V
  - **vih range** - 0 to 7.1V
  - **vol range** - 0 to +5V
  - **voh range** - 0 to +5V
  
- **Driver Specification**
  - **min pulse width (3V)** - 3ns
  - **rise/fall time (3V)** - 1.9ns
  - **Edge accuracy** -  $\pm 500$  ps
  
- **Per Pin Measurement Unit**
- **High Voltage pin**
  - 4 pins per board (0 to +16V)

## FLEX

### • Digital channel

- **Channels per board** – 48 channels
- **Maximum Large vector memory** – 64 Meg
- **Maximum board per tester** – 24
- **Maximum channels per tester** – 1152
- **Maximum vector rate** – 200Mhz
  
- **Pin Level**
  - **vil range** - -1 to + 6V
  - **vih range** - -1 to 6V
  - **vol range** - -1 to + 6V
  - **voh range** - -1 to + 6V
  
- **Driver Specification**
  - **min pulse width (3V)** –2.2ns
  - **rise/fall time (3V)** - 1.5ns
  - **Edge accuracy** -  $\pm 250$  ps
  
- **Per Pin Measurement Unit**
- **High Voltage pin**
  - 2 pins per board (0 to +20V)



## J750

- **Memory Test Option (MTO)**

**per board**

- **50 MHz** execution rate
- **8M 48-bit word Capture Memory**
- Algorithmic Pattern Generator
- 2 X 16-bit address generators (X+Y)
- 2 data generators:
  - (2) 1-bit and (1) 16-bit
- 2 Scramble RAMs
- Topological inversion
- 512K x 16 Fail Map Memory

## FLEX

- **Memory Test Option (MTO)**

**per board**

- **100MHz** execution rate
- **24M 64-bit word Capture Memory**
- Algorithmic Pattern Generator
- 4 X 16-bit address generators (X+Y)
- 4-bit Z address generator
- 2 data generators:
  - (2) 1-bit and (1) 32-bit
- 2 Scramble RAMs
- Topological inversion
- 1M x 32 Fail Map Memory



# High Speed Digital – Power Supply

## J750

- **Digital Power Supply (DPS)**
- **Digital Power Supply**
  - 8 Channel V/I per board
  - 0V to 10V 1A per channel
  - Max 4 board per tester
  - Max 32 power supply per tester

## FLEX

- **DC and Power Supply**
- **Power Supply - DC30**
  - 20 Channel V/I with Meter per Channel
  - +/- 30V, 100mA or +/-10V, 200mA per channel
  - Functional DC source and measurement
- **Per-Pin Power Resource DC75**
  - 4 Channel V/I with Meter per Channel
  - +/- 75V, 350mA to +/-6V, 2A per channel
  - Functional DC source and measurement
- **Per-Pin High Power Resource DC90**
  - 4 Floating V/I with Meter per Channel
  - 25V 20A or 180V 500mA pulsed
  - Functional DC source and measurement
- **Per-Pin High Power Resource HexVS**
  - 6 High Current Voltage Sources with Meter per Channel
  - 5.5V 15A, Merge able to 90 A @ 3.6V
  - Current Profiling
  - Fast current transition response

# High Speed Digital – Mixed Signal Option

## J750

- **Mixed Signals Instrument**

- **Mixed Signal Options (MSO)**

- **4 Sources and 4 Captures per board**

- **Source**

- 16 Meg source memory

- LF to 20 KHz (SINAD 100dB)

- HF to 23 MHz (SINAD 52 dB)

- **Capture**

- 32 Meg capture memory

- LF to 20 KHz (SINAD 100dB)

- MF to 6 MHz (SINAD 74 dB)

- **Converter Test Option (CTO)**

- **8 instruments per board**
- **Max. 4 board per tester (32 instr max.)**
- **Voltage range** - 0 to 6V and 0 to 3V ranges
- 14 bit accuracy (16 bit resolution)
- 2 Reference voltage sources
- Pattern Generator controlled
- Optimized for Linearity testing of A/Ds

## FLEX

- **Mixed Signals Instrument**

- **Boardband AC (BBAC)**

- **2 AWGs and 2 digitizers per board**

- Bandwidth - 15MHz

- -154 dB/Hz noise floor

- -120 dB THD, -114 dB SNR

- PPMU per channel

- Single-ended or differential

- **VHFAC**

- **2 AWGs and 2 digitizers per board**

- **Sources**

- 400MS/s Sampling Rate

- 8M sample Waveform Memory

- 75dB Harmonics and Spurs @ 1Mhz

- **Digitizer**

- DC to 32.5 MHz, 14 bits

- DC to 62.5 MHz, 12 bits

- Under sampling: DC to 300MHz

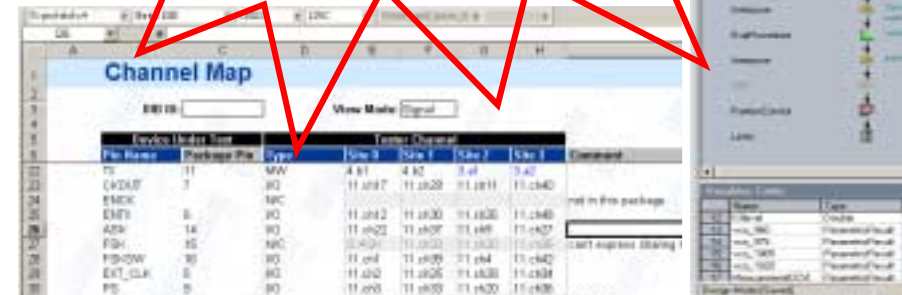
- -75dB Harmonics and Spurs @ 1Mhz

- 1 Mega-sample capture memory


# Software - IG-XL

- Excel Spreadsheet based environment
- GUI Based Code Debug/Development environment
- VBT Code environment

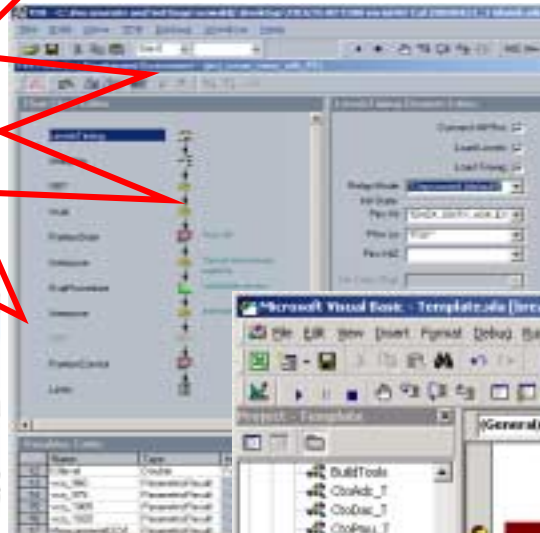
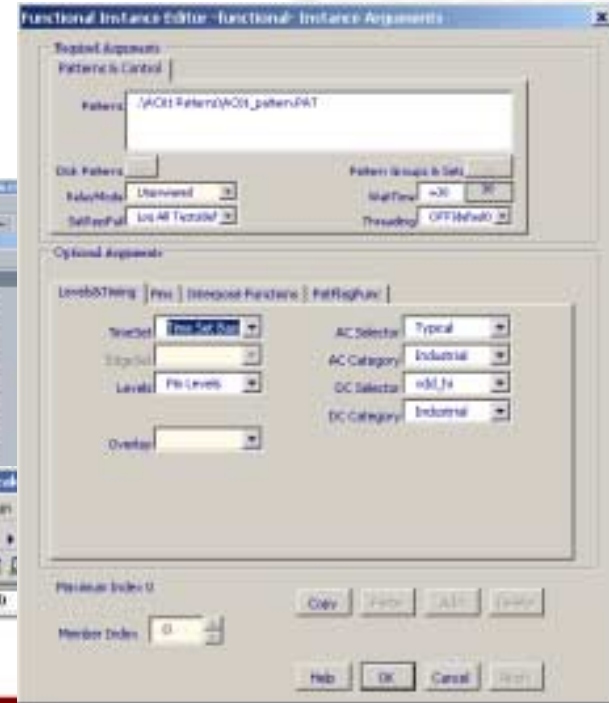
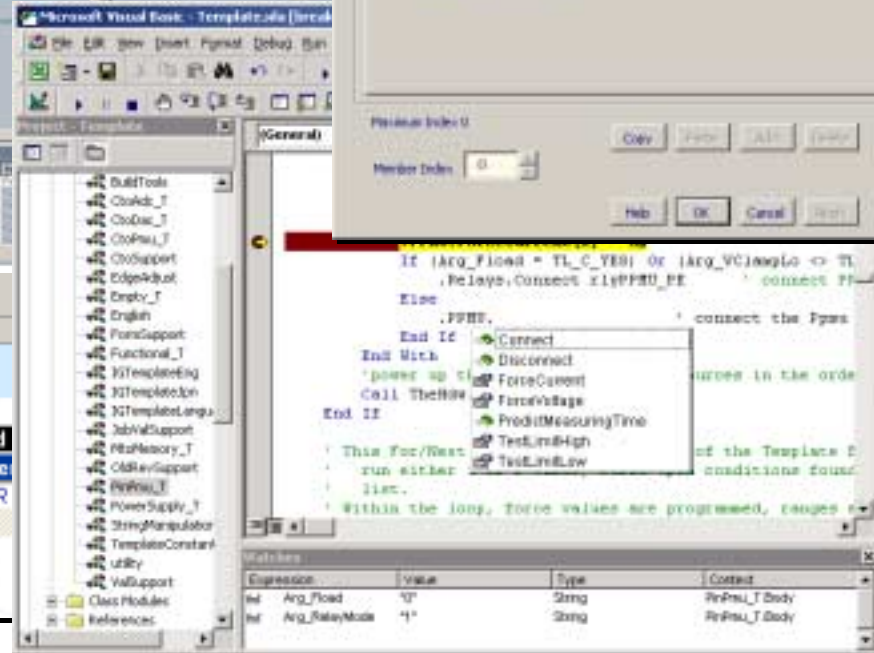
**Same IG-XL software environment is used for both J750 and FLEX**



Pin Name	Package Pin	Type	Site 1	Site 2	Site 3	Site 4	Comment
TS	11	MW	4 81	4 82	3 41	3 42	
CKOUT	7	8Q	11 2817	11 2829	11 2811	11 2840	
EMCK	3	8Q					not in pin package
EMF1	8	8Q	11 2812	11 2830	11 2826	11 2846	
AD1	14	8Q	11 2822	11 2827	11 2819	11 2827	
FBI4	15	8Q	11 2824	11 2823	11 2823	11 2825	
FB-DW	30	8Q	11 2814	11 2829	11 2814	11 2842	
EXT_CLK	5	8Q	11 2810	11 2825	11 2838	11 2834	
PS	9	8Q	11 2810	11 2829	11 2820	11 2836	
WLS_Pack	9	DCVt	3 41	3 42	3 41	3 42	VDD 2P

Label	Enable	Gate			Command	
		Job	Part	Env	Opcode	Parameter
					Test	IC_SNR
					stop	

```

IF (Arg_Flow = TL_C_YES) OR (Arg_VC[angle] <> TL
, Relays.Connect x1[PPDU_PE] connect PP
Else
.PPDU. connect the Pps
End If
End With
power up tl ForceCurrent sources in the orde
Call TheHW ForceVoltage
End If
Prod(MeasuringTime
Test(LimHigh of the Template f
run either Test(LimLow conditions four
list. Within the loop, force values are programmed, ranges

```

Expression	Value	Type	Context
Arg_Flow	'0'	String	RePsi_T_Body
Arg_RelayMode	'1'	String	RePsi_T_Body

# Software – OS platform and IG-XL version

## J750

## FLEX

### IG-XL version

Latest release IG-XL 3.40.11

### OS software

Offline

Windows NT  
Windows 2000 (V3.30.00 or higher)  
Windows XP (V3.40.09 or higher)

Online

Windows NT  
Windows 2000 (V3.40.00 or higher)  
Windows XP (V3.40.09 or higher)

### Microsoft office

Office 97  
Office 2000 (v3.40.00 or higher)  
Office XP (v3.40.09 or higher)

### IG-XL version

Latest release IG-XL 5.00.60

### OS software

Offline

Windows 2000  
Windows XP

Online

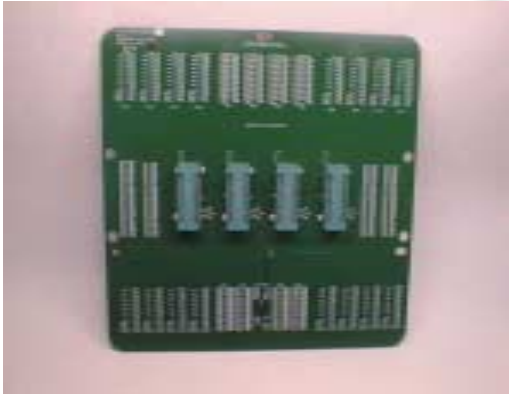
Windows 2000  
Windows XP

### Microsoft office

Office 2000  
Office XP

# Software – channel map differences

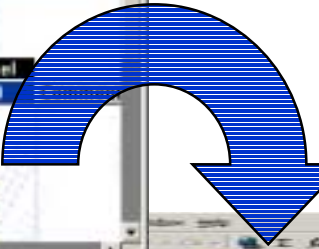
J750



Channel Map

DIB ID:

Device Under Test		Tester Channel	
Pin Name	Package Pin	Type	Site ID
p1a	1	VO	ch41
p1b	2	VO	ch42
p1y	3	VO	ch44
p2a	4	VO	ch46
p2b	5	VO	ch47
p2y	7	VO	ch45



Minor channel map modification due to DIB hardware difference.

FLEX

Channel Map

DIB ID:

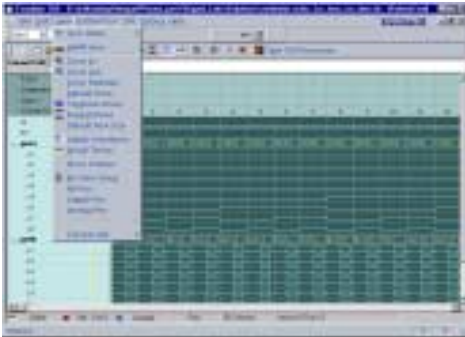
Device Under Test		Tester Channel		View Mode	Pop
Pin Name	Package Pin	Type	Site ID	Pop	Comment
a1	1	VO	11.a15	Good	
a2	2	VO	11.a17	Good	
a3	3	VO	11.b15	Good	
a4	4	VO	11.b16	Good	
a5	5	VO	11.b18	Good	
a6	6	VO	11.c11	Good	
a7	7	VO	11.b15	Good	
a8	8	VO	11.c14	Good	
a9	9	VO	11.c16	Good	
a10	10	VO	11.c18	Good	
a11	11	VO	11.c19	Good	
a12	12	VO	11.c20	Good	
a13	13	VO	11.b20	Good	
a14	14	VO	11.c20	Good	
a15	15	VO	11.c20	Good	
a16	16	VO	11.c20	Good	
a17	17	VO	11.c20	Good	
a18	18	VO	11.c20	Good	
a19	19	VO	11.c20	Good	
a20	20	VO	11.c20	Good	
a21	21	VO	11.c20	Good	
a22	22	VO	11.c20	Good	
a23	23	VO	11.c20	Good	
a24	24	VO	11.c20	Good	
a25	25	VO	11.c20	Good	
a26	26	VO	11.c20	Good	
a27	27	VO	11.c20	Good	
a28	28	VO	11.c20	Good	
a29	29	VO	11.c20	Good	
a30	30	VO	11.c20	Good	
a31	31	VO	11.c20	Good	
a32	32	VO	11.c20	Good	
a33	33	VO	11.c20	Good	
a34	34	VO	11.c20	Good	
a35	35	VO	11.c20	Good	
a36	36	VO	11.c20	Good	
a37	37	VO	11.c20	Good	
a38	38	VO	11.c20	Good	
a39	39	VO	11.c20	Good	
a40	40	VO	11.c20	Good	
a41	41	VO	11.c20	Good	
a42	42	VO	11.c20	Good	
a43	43	VO	11.c20	Good	
a44	44	VO	11.c20	Good	
a45	45	VO	11.c20	Good	
a46	46	VO	11.c20	Good	
a47	47	VO	11.c20	Good	
a48	48	VO	11.c20	Good	
a49	49	VO	11.c20	Good	
a50	50	VO	11.c20	Good	
a51	51	VO	11.c20	Good	
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a77	77	VO	11.c20	Good	
a78	78	VO	11.c20	Good	
a79	79	VO	11.c20	Good	
a80	80	VO	11.c20	Good	
a81	81	VO	11.c20	Good	
a82	82	VO	11.c20	Good	
a83	83	VO	11.c20	Good	
a84	84	VO	11.c20	Good	
a85	85	VO	11.c20	Good	
a86	86	VO	11.c20	Good	
a87	87	VO	11.c20	Good	
a88	88	VO	11.c20	Good	
a89	89	VO	11.c20	Good	
a90	90	VO	11.c20	Good	
a91	91	VO	11.c20	Good	
a92	92	VO	11.c20	Good	
a93	93	VO	11.c20	Good	
a94	94	VO	11.c20	Good	
a95	95	VO	11.c20	Good	
a96	96	VO	11.c20	Good	
a97	97	VO	11.c20	Good	
a98	98	VO	11.c20	Good	
a99	99	VO	11.c20	Good	
a100	100	VO	11.c20	Good	



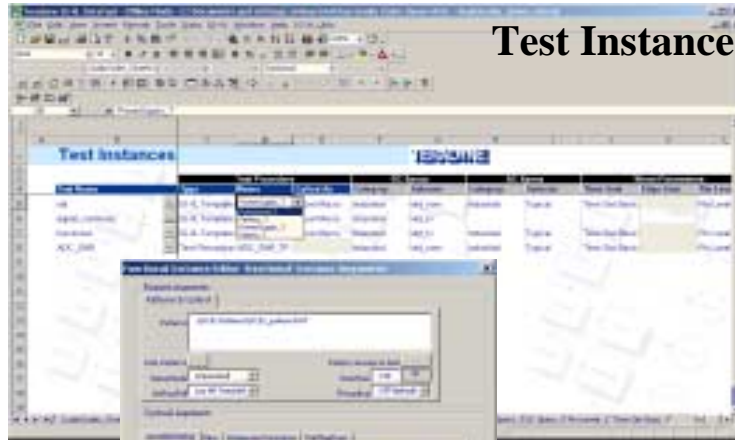
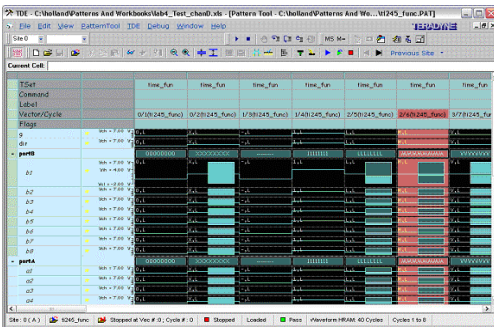
# Software - IG-XL (FLEX Debug tools)

More extensive debug tools available on FLEX

Pattern Tool II



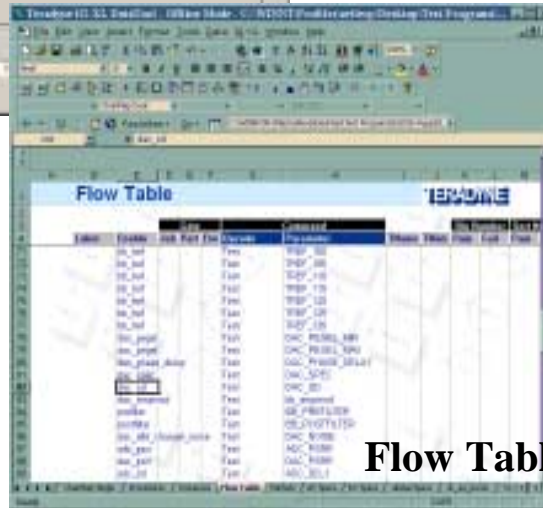
HRAM Pattern Tool



Test Instance



Test Template



Flow Table

Test Debug Environment



VBA Debug

