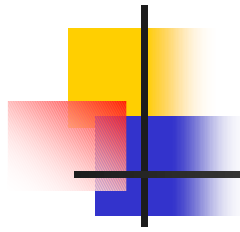




Memory

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Adapted from EE271 notes,
Stanford University

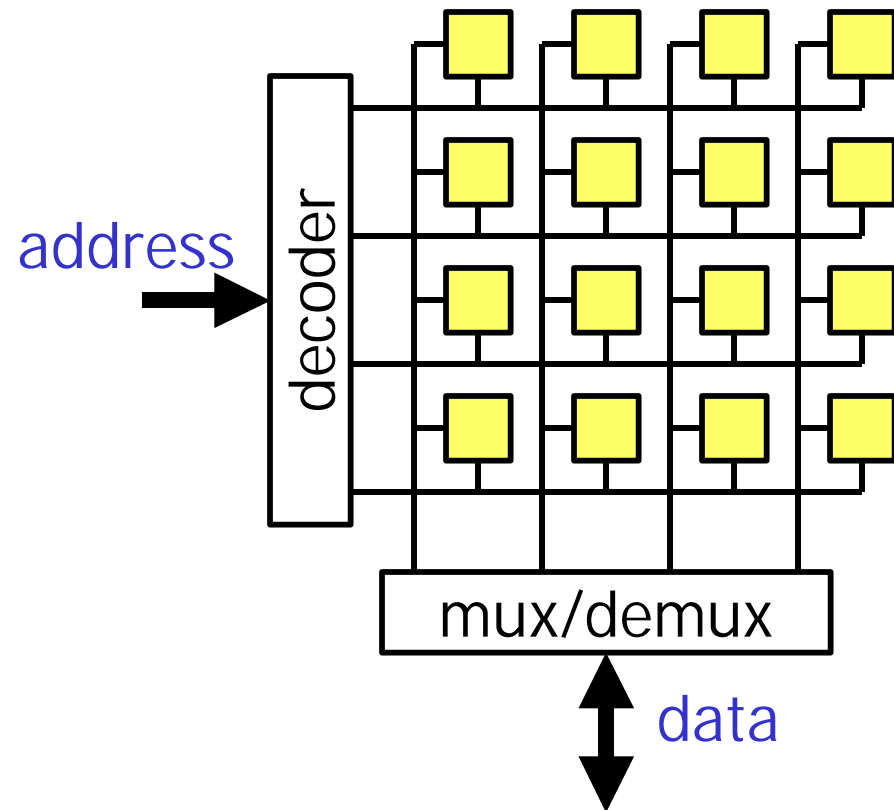


Overview

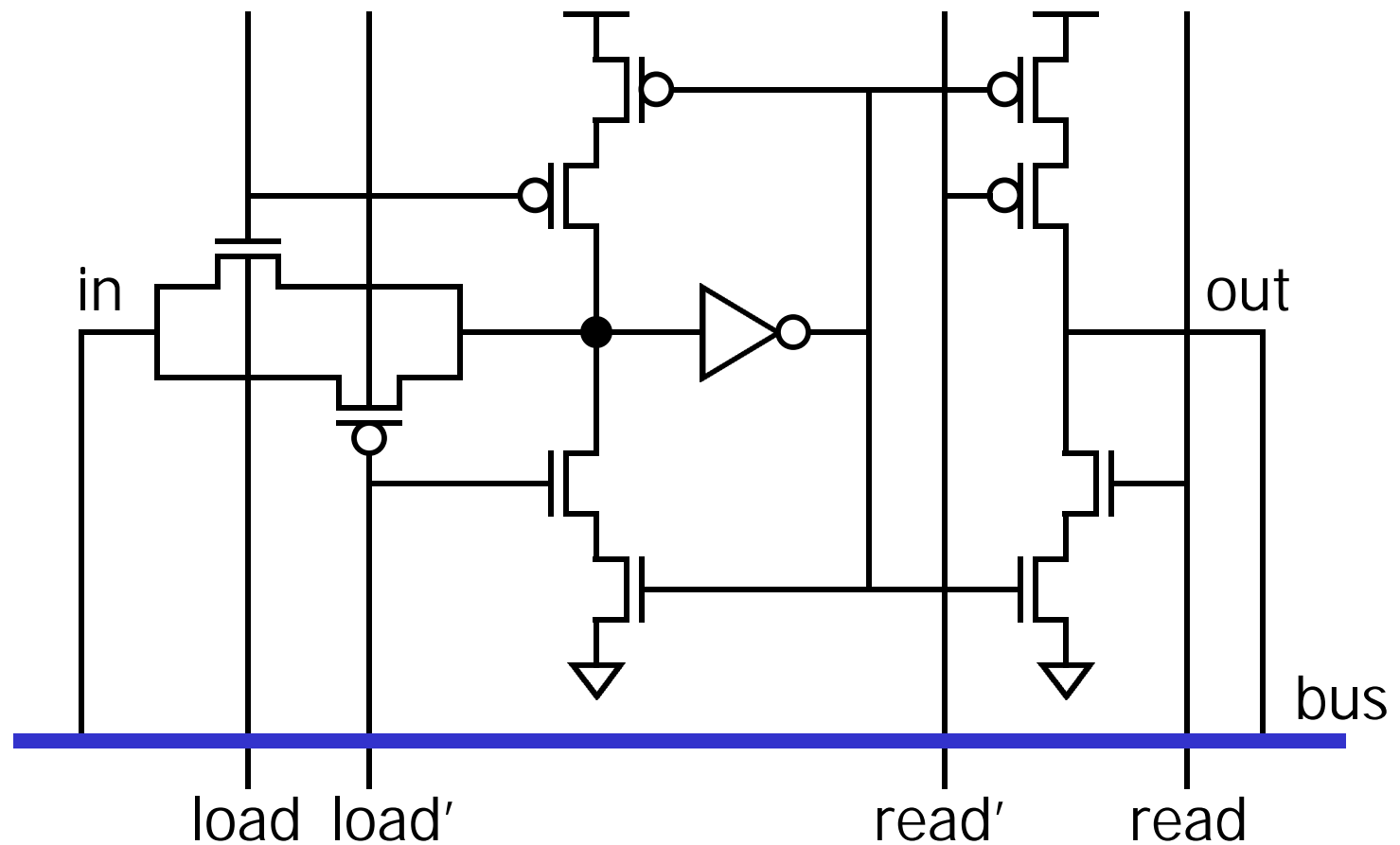
- Static random access memory (SRAM)
- Dynamic random access memory (DRAM)
- Content addressable memory (CAM)
- Reading
 - W&E 8.3.1-8.3.2

Memory Array

- Structured wiring
- Dense layout
- N^2 elements but only $2N$ wires



Basic Latch Cell



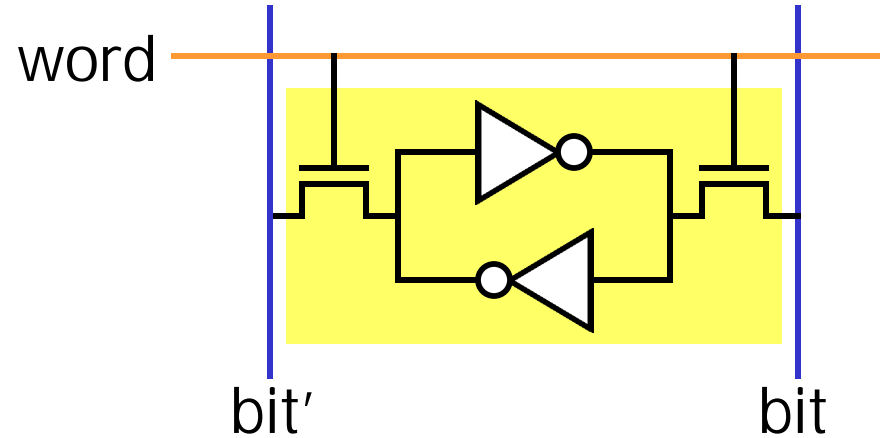
- Large number of control wires required
- Cell size becomes large



Memory Cell Design

- Memory array typically needs to store lots of bits
 - Need to/can afford to optimize cell design for area and performance
 - Peripheral circuits can be complex
 - Much smaller compared to the array
- Memory cell design
 - 6T cell (most common)
 - 4T cell with poly load
 - 1T DRAM cell

6T SRAM Cell



- Data stored in cross-coupled inverters
- One **word** line and two **bit** lines
 - Cell enabled when **word** = 1
 - **Bit** lines carry data
 - Same port for read and write

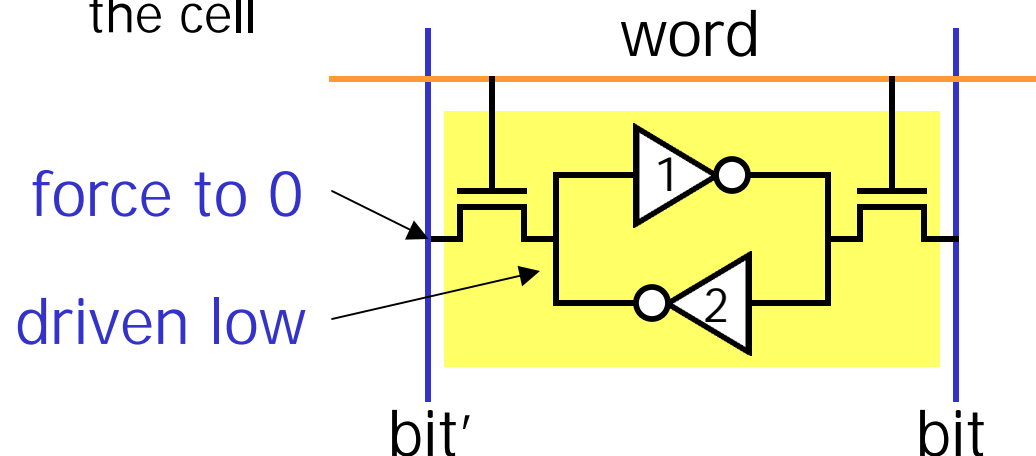
6T SRAM Cell Operations

■ Read operation

- Both bit and bit' are precharged high
- When cell enabled
 - bit' discharged if 1 had been stored in the cell
 - bit discharged if 0 had been stored in the cell

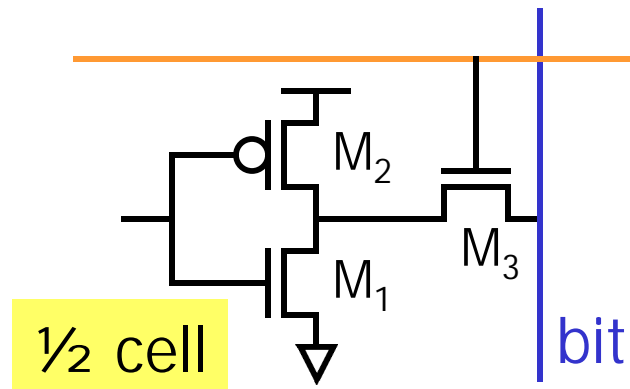
■ Write operation

- To write 1, force bit' to 0
 - which overpowers INV#2's pMOS
 - and drives INV#1's output high, latching 1 in the cell

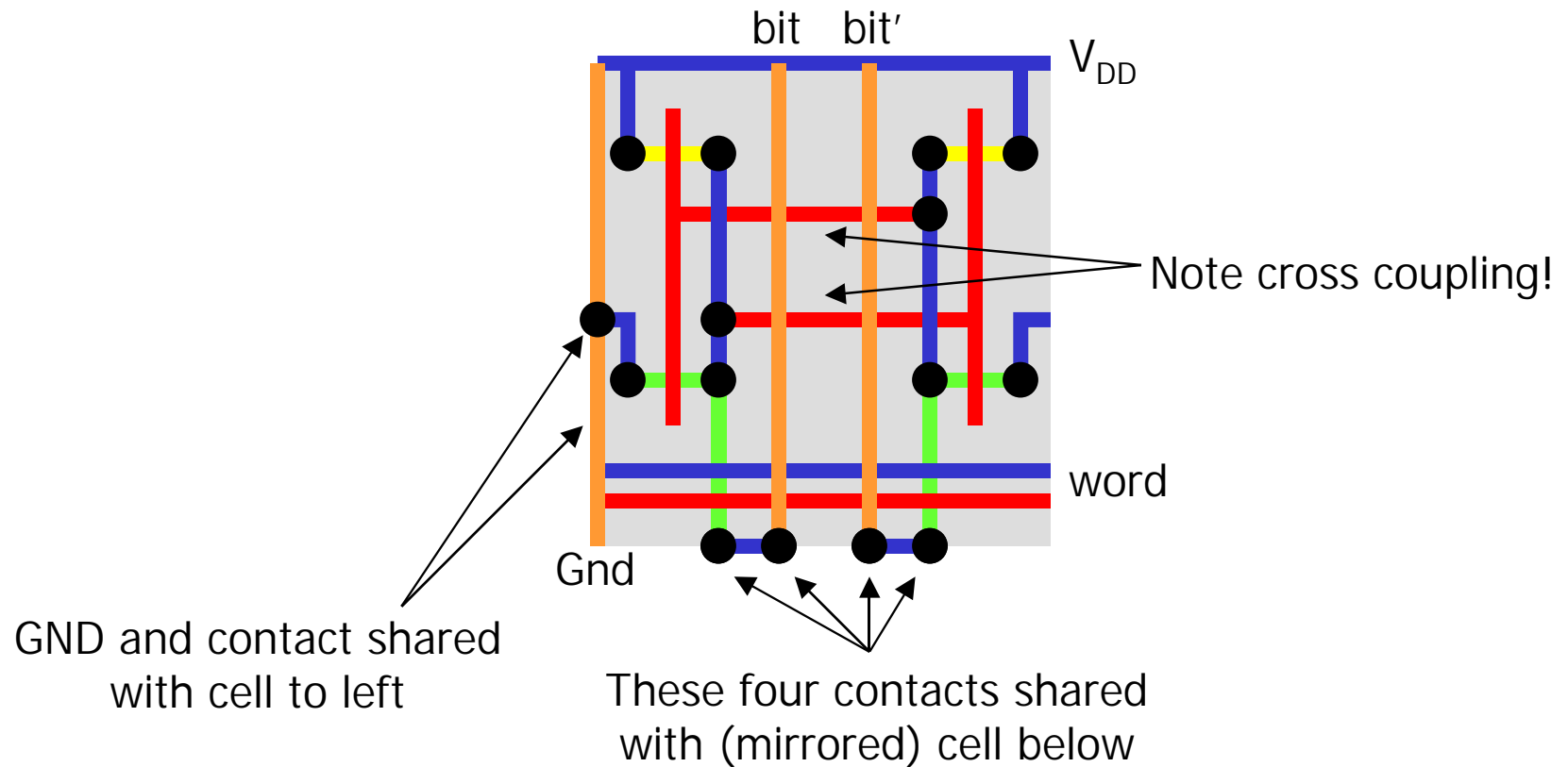


SRAM Cell Design

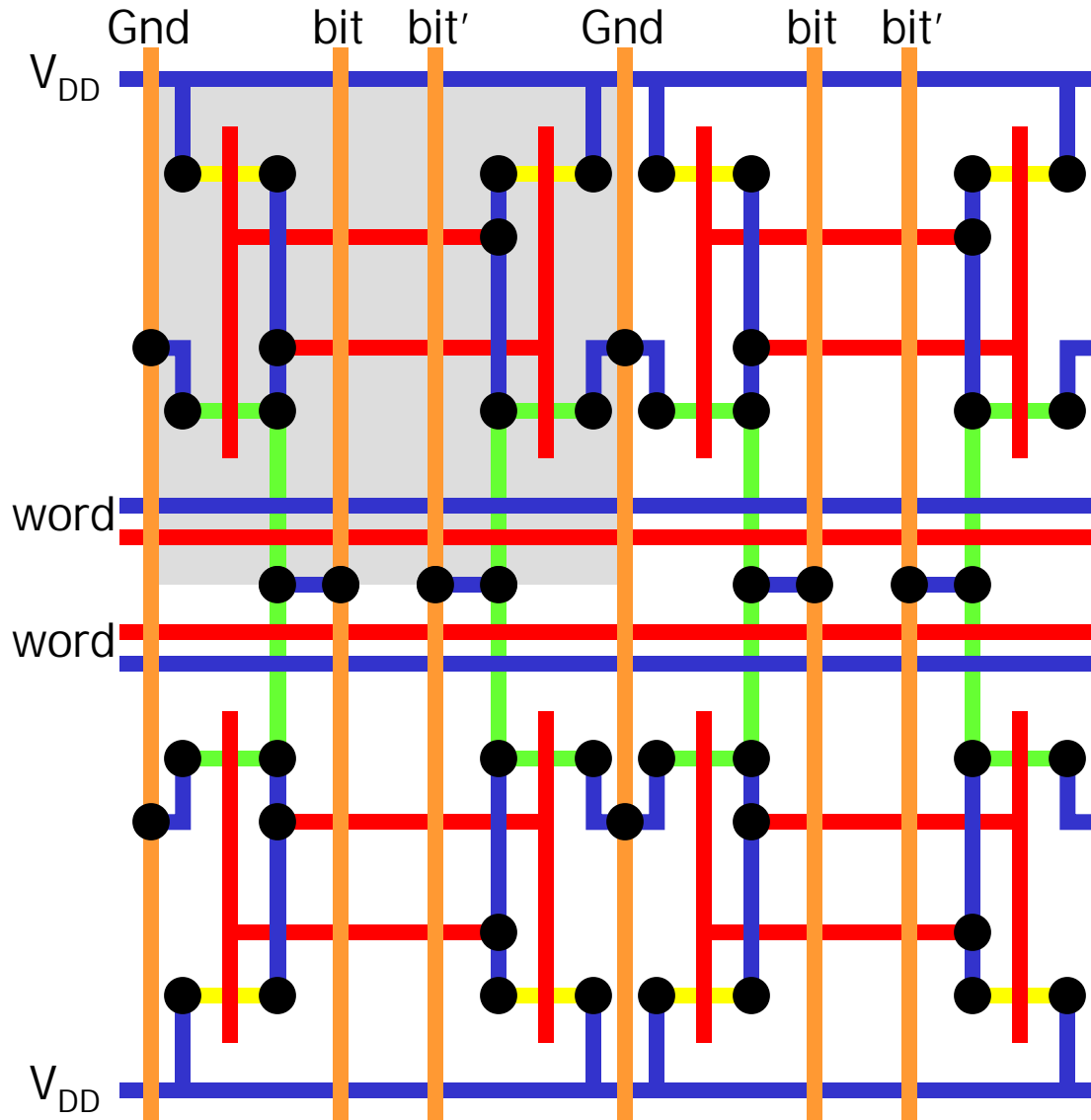
- For the cell to work correctly,
 - 0 on the bit line must overpower M_2 during write
 - M_3 must be at least $1.5 \times M_2$
 - At the same time, M_1 must be able to pull bit down during read
 - M_1 must be at least $1.5\text{-}2 \times M_3$



SRAM Cell Layout

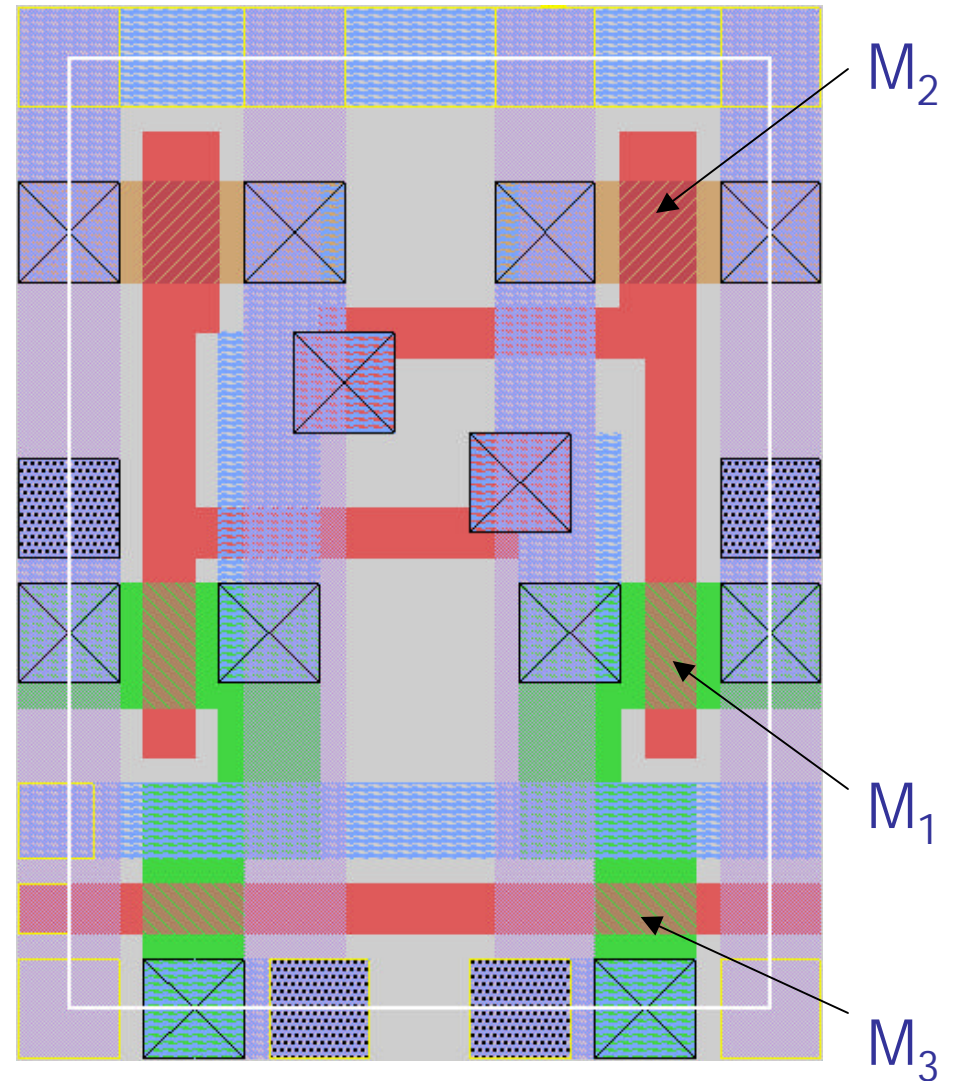


SRAM Cell Layout (2x2)

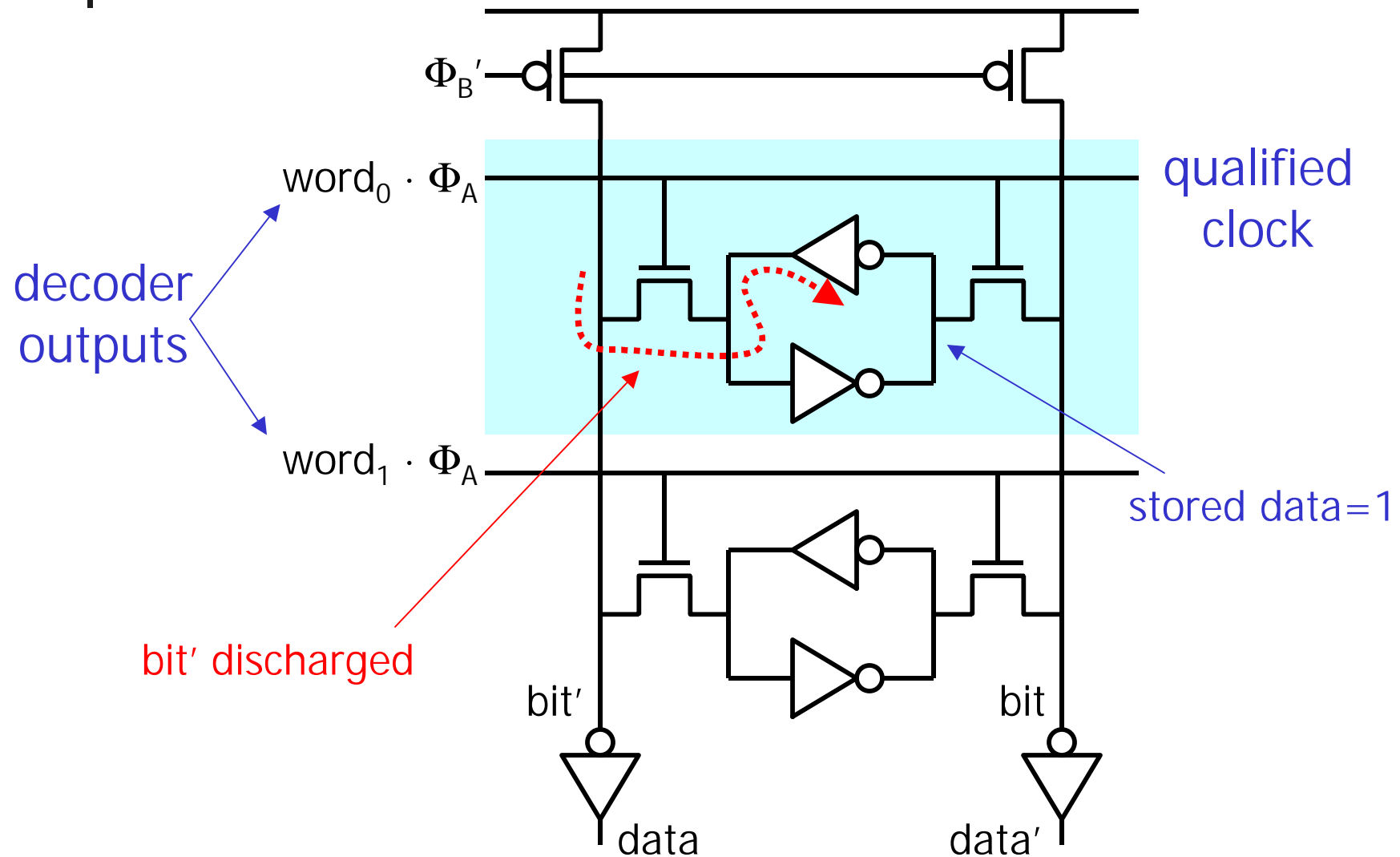


6T SRAM Cell Layout

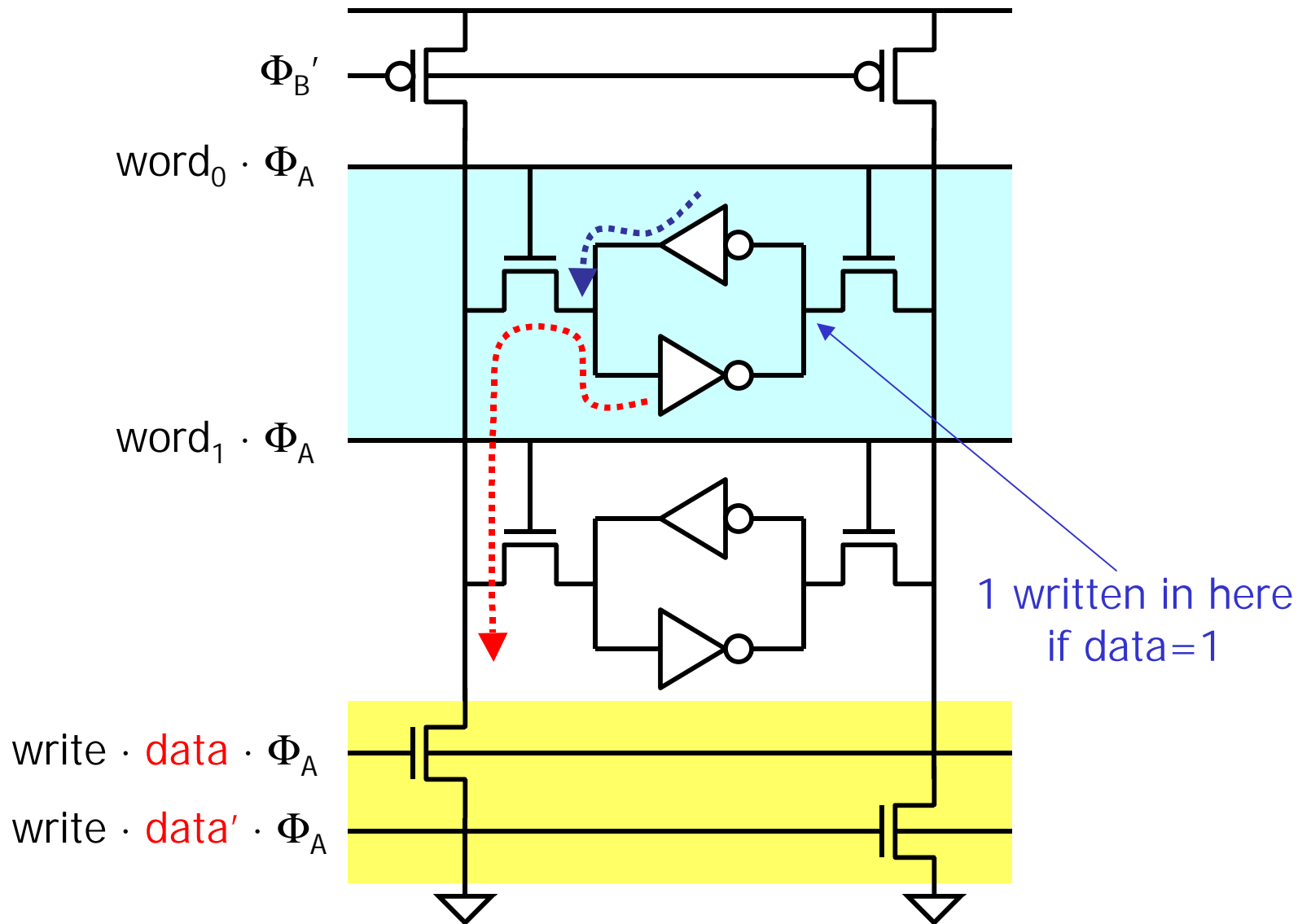
- Transistor sizing
 - M_2 (pMOS) 4:3
 - M_1 (nMOS) 6:2
 - M_3 (nMOS) 4:2
- All boundaries shared
- 38λ H x 28λ W
 - about $\frac{1}{4}$ of latch cell size
- Reduced cap on bit lines



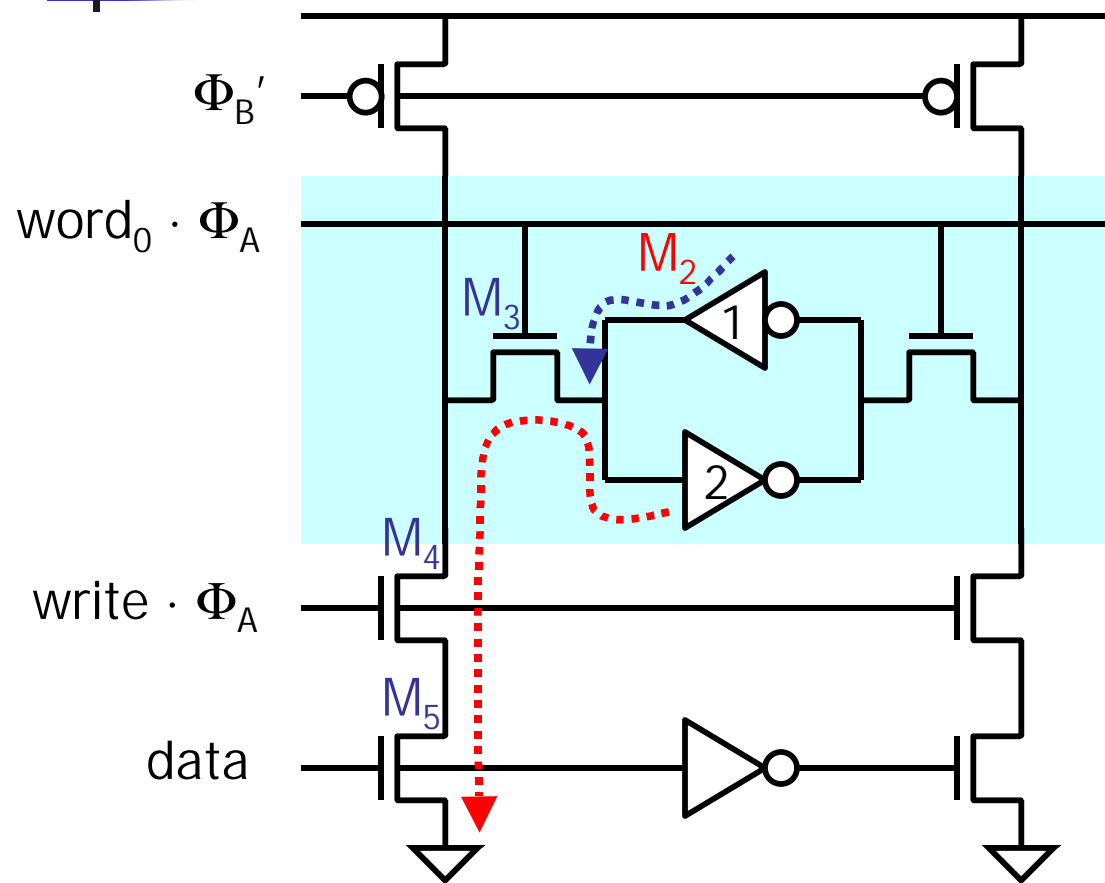
Bit Line I/O (Read)



Bit Line I/O (Write I)

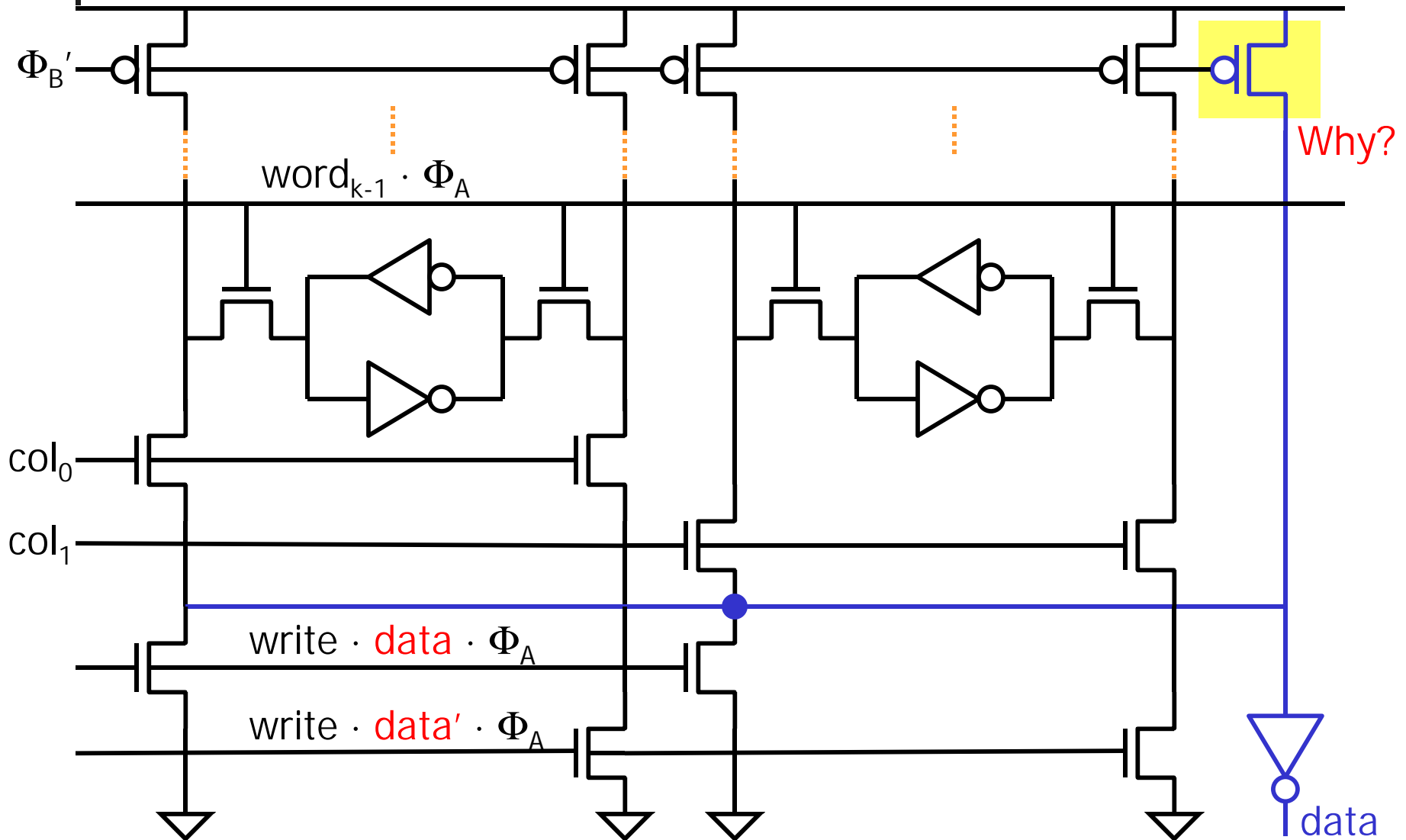


Bit Line I/O (Write II)

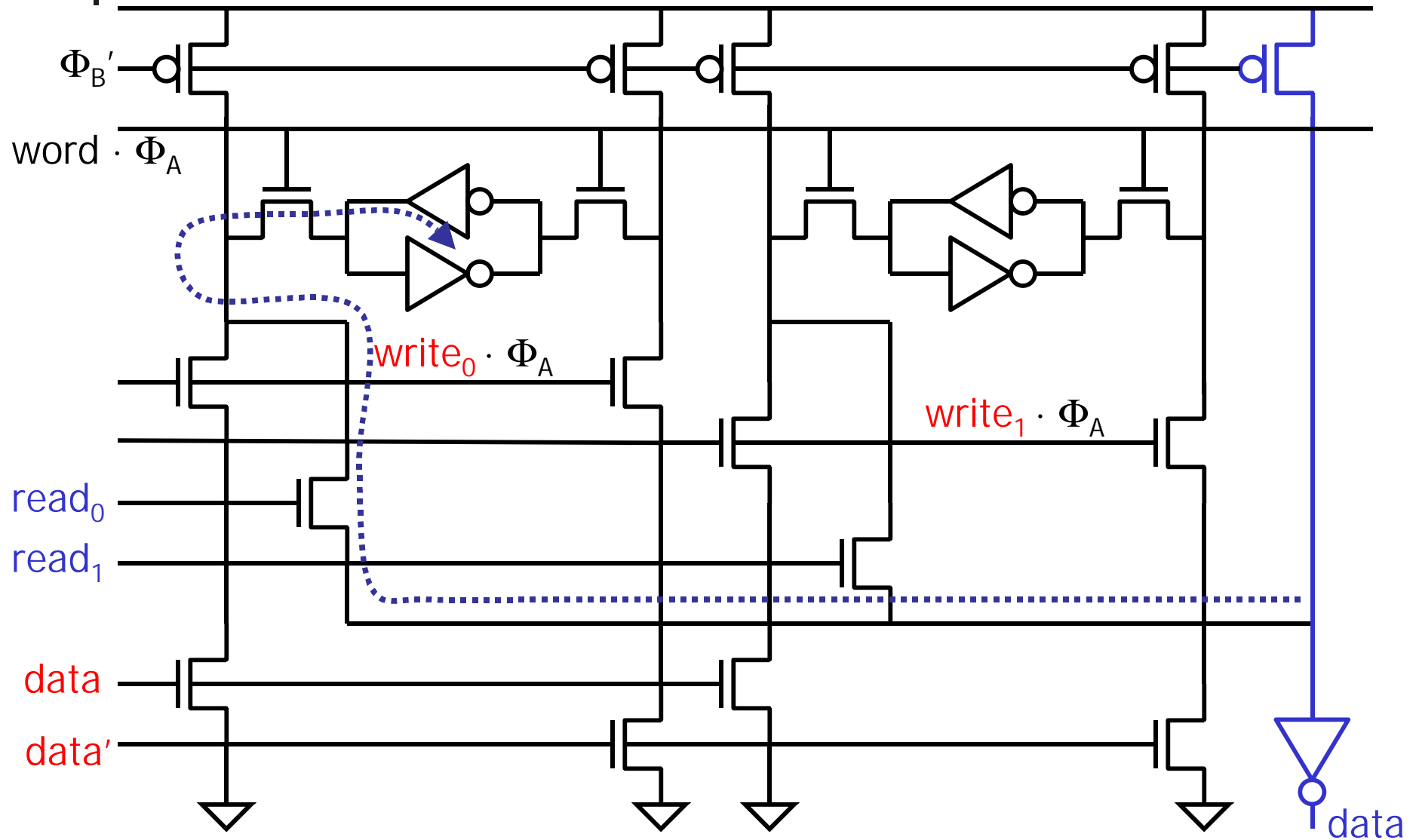


- $R_3 + R_4 + R_5$ should be $< \frac{1}{2}R_2$
- If $M_2 = 4:3$ and $M_3 = 4:2$, then $\frac{1}{2}R_2 = \frac{3}{4}R_{\bullet}$ and $R_3 = \frac{1}{2}R_{\bullet}$; therefore $R_4 + R_5$ should be $R_{\bullet}/4$
 - I.e., M_4 and M_5 should be 16:2 each

Bit Line Multiplexing I



Bit Line Multiplexing II



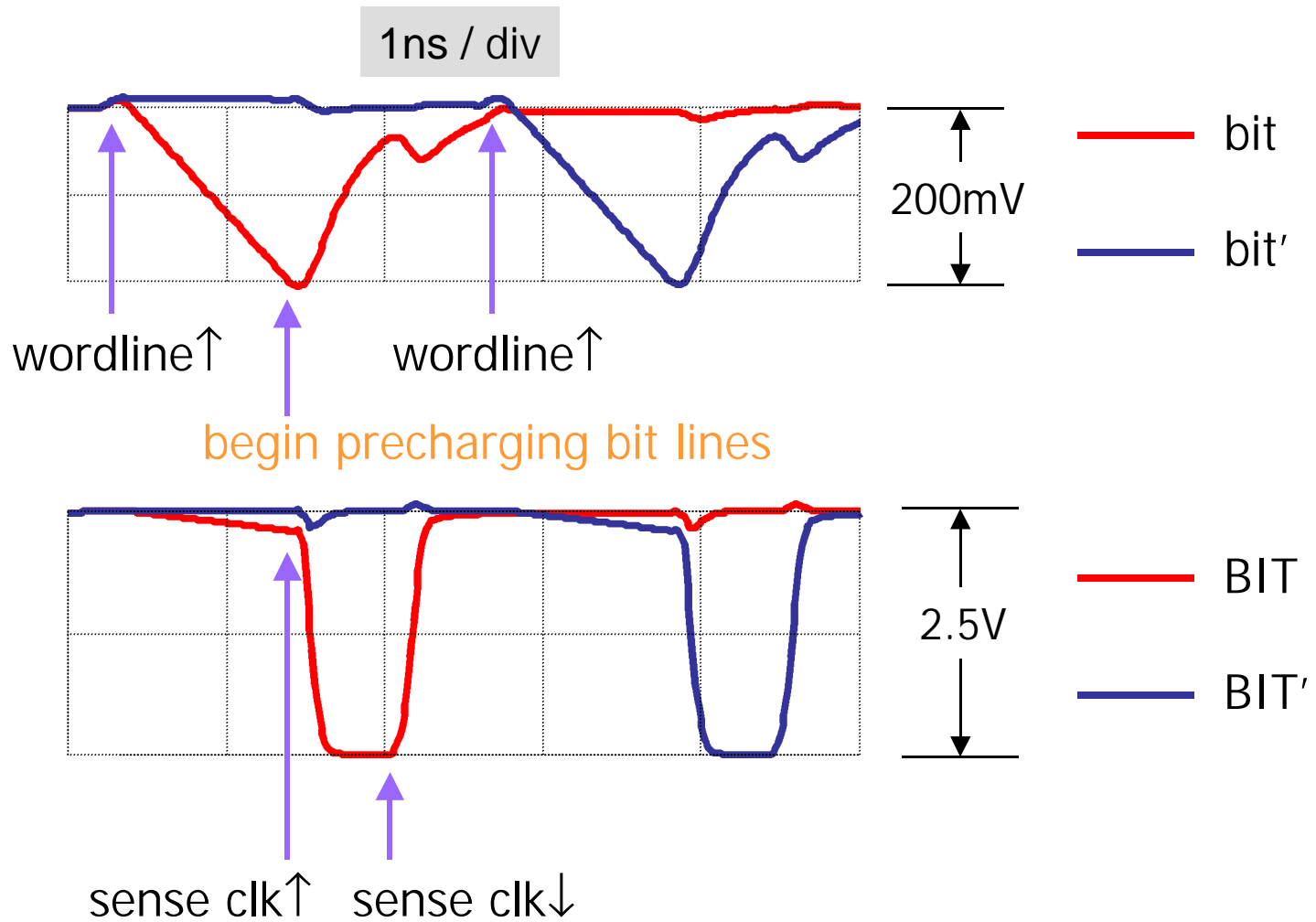


Sense Amplifier: Why?

- Bit line cap significant for large array
 - If each cell contributes 2fF,
 - for 256 cells, 512fF plus wire cap
 - Pull-down resistance is about 15K
 - $RC = 7.5\text{ns!}$ (assuming $\Delta V = V_{dd}$)
- Cannot easily change R, C, or V_{dd} , but **can** change ΔV !
 - Can reliably sense ΔV as small as 50mV
 - With margin for noise, most SRAMs sense bit-line swings between 100~300mV
 - For writes, still need to drive the bit line full-swing (all the way to Gnd)
 - only one driver needs to be this big

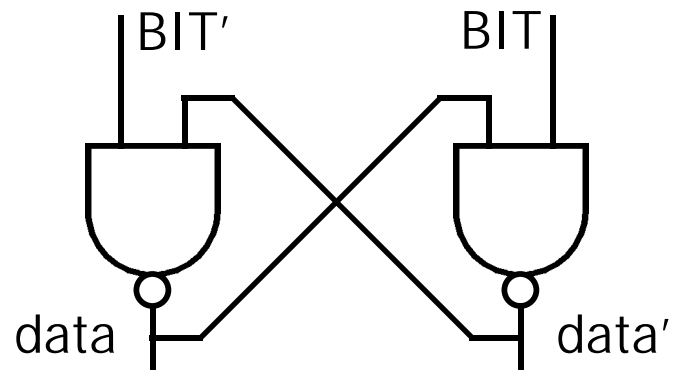
$$t = \frac{RC\Delta V}{V_{dd}}$$

Sense Amp Waveforms



Sense Amp (Caveat I)

- Isolation transistors must be pMOS
 - Bit lines are within 0.2V of V_{dd} (not enough to turn nMOS on)
- Load on outputs of regenerative amplifier must be equal
 - Both outputs go high during precharge
 - Usually follow regenerative amplifier by cross-coupled NAND latch

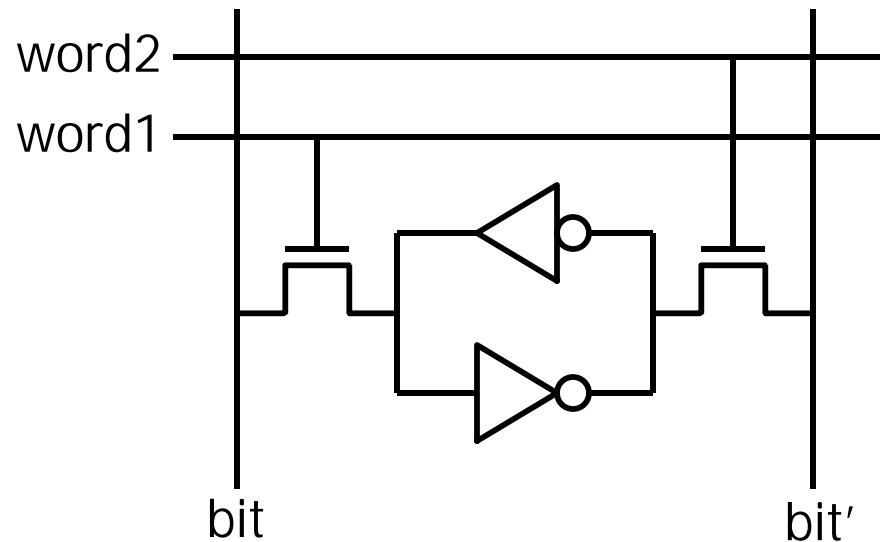




Sense Amp (Caveat II)

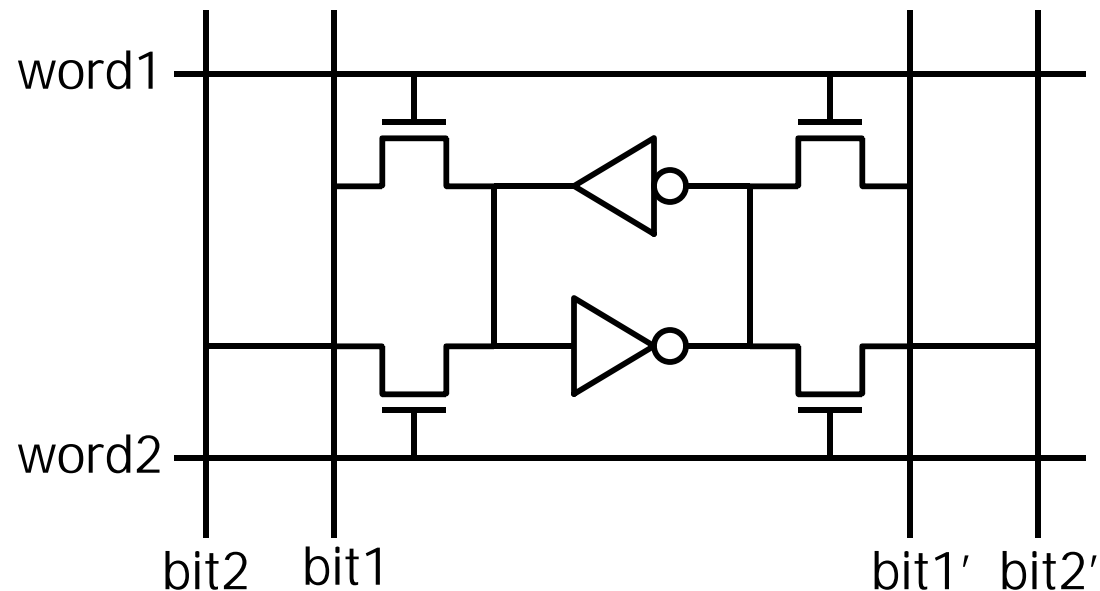
- For SRAM, one S/A for 4-8 columns
 - after column mux
- For DRAM, one S/A for every column
 - for refresh!
- Need to precharge S/A before opening isolation transistors
 - To avoid discharging bit lines
 - Requires 3 timing phases
 - Typically self-timed

Dual-Port SRAM Cell

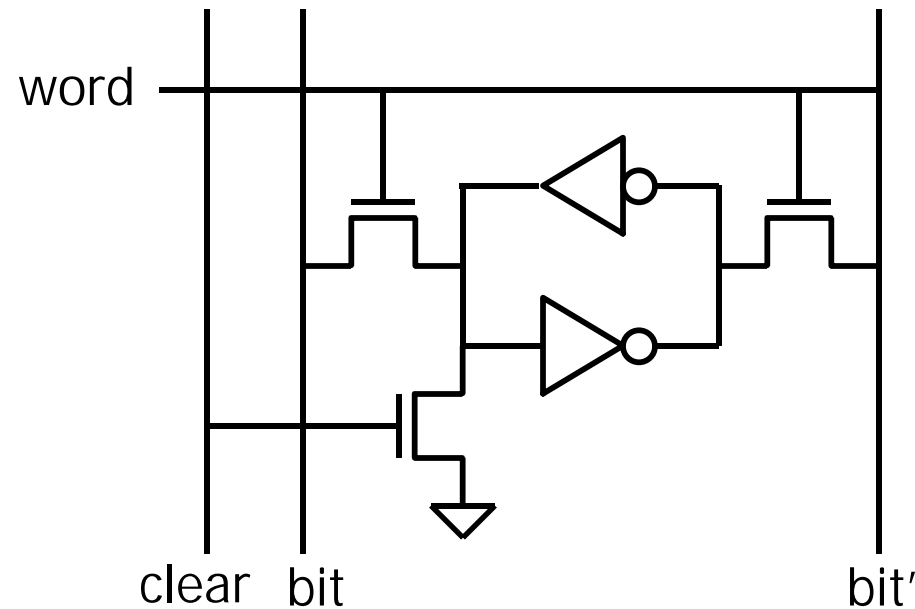


- Two single-rail read ports
- One write port
 - Both word1 and word2 must be asserted together

Full Dual-Port SRAM Cell

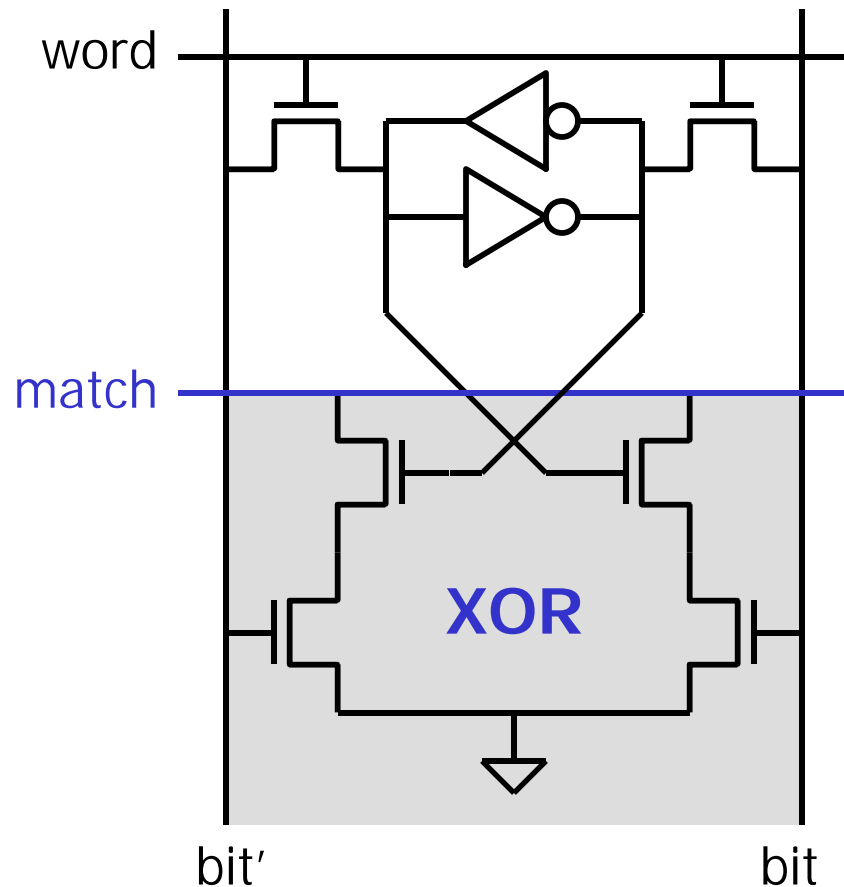


- Two word lines and four bit lines
- Can independently select two rows for read or write
- Often used for FIFO



- Asserting **clear** resets all the bits in a column in one shot
- Often used to clear valid bits in caches and TLB's

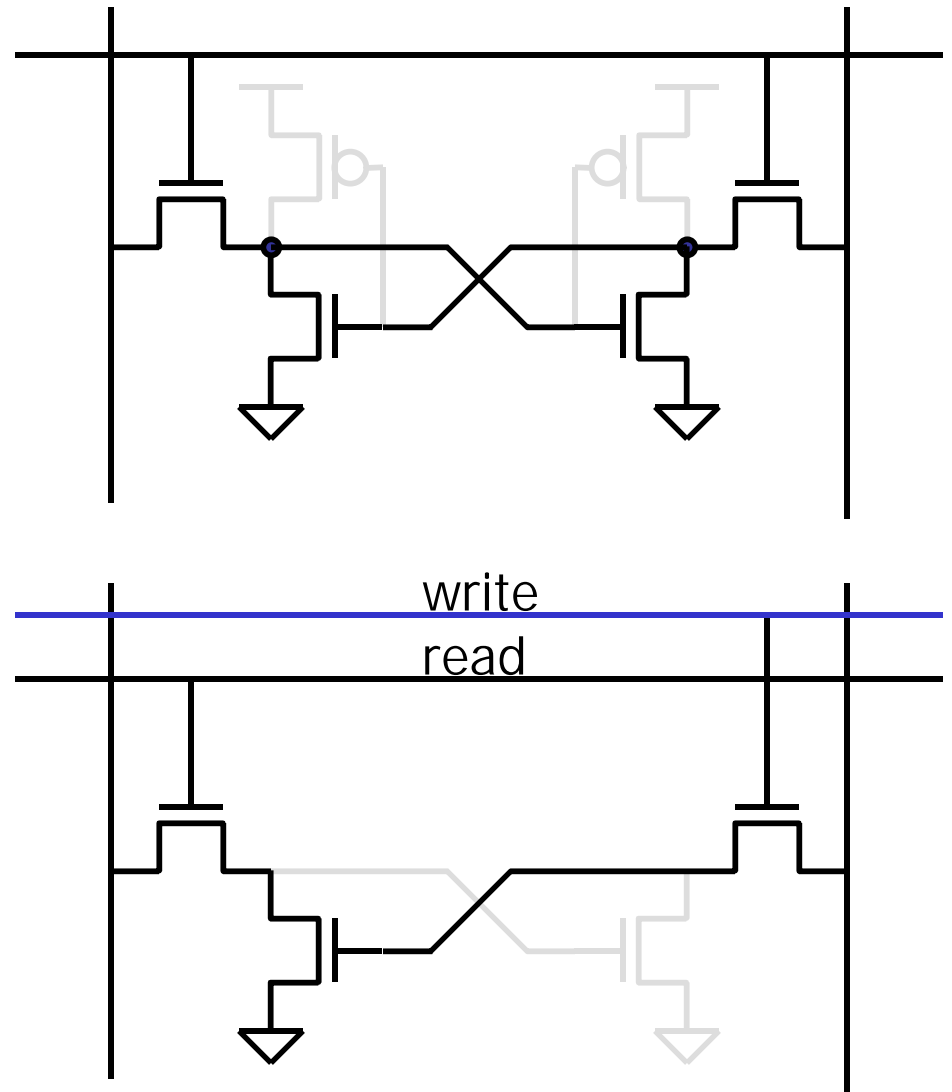
Content Addressable Memory (CAM) Cell



- When word asserted,
 - Functions like a conventional RAM cell
- When word not asserted,
 - Cell content compared to bit
 - In case of mismatch, precharged **match** line discharged
- Connect all the bits to match line
 - Match line remains high only if every bit matches
 - Can we have **don't cares**?

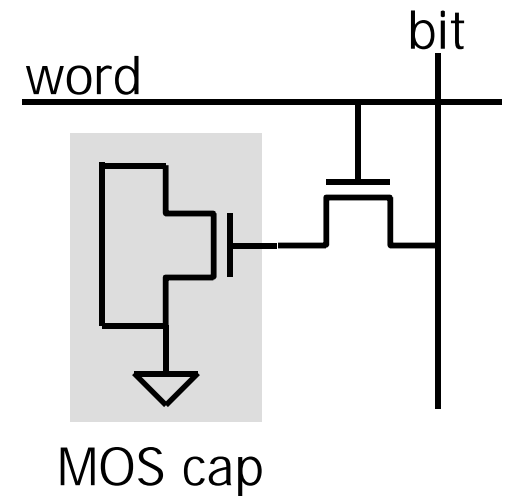
4T/3T DRAM Cell

- Cell smaller but difficult to design
 - Dynamic storage (no pMOS pull-up)
 - Logic 1 degraded
 - nMOS pull-downs have weaker drive
 - V_{dd} must be high enough
- 3T design: single rail
 - Two wordlines: one for read; one for write
 - Not much smaller than 4T
 - Only interesting historically: used in Intel 1103 DRAM

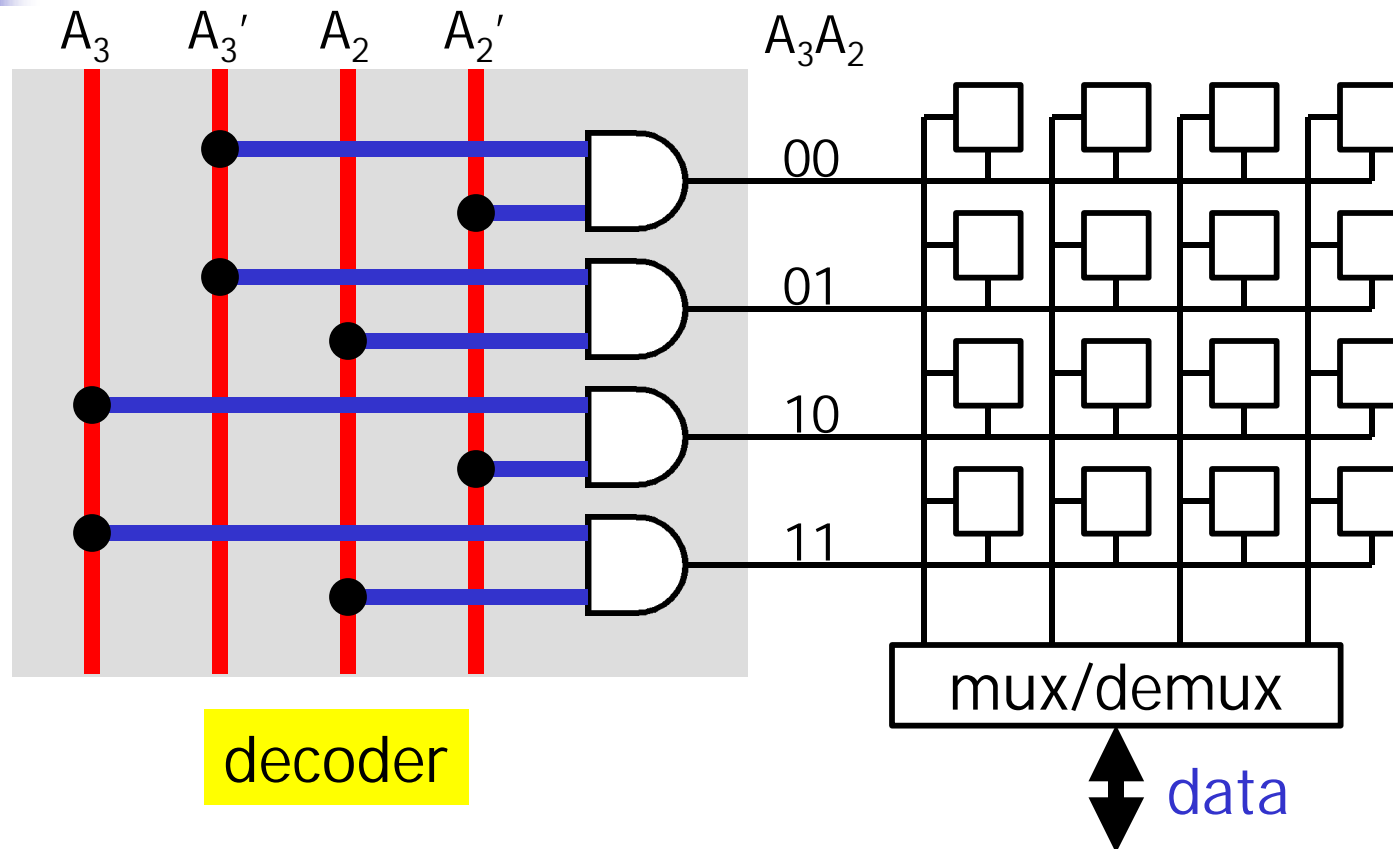


1T 1R DRAM Cell

- To write
 - Assert wordline and drive 1 or 0 on bitline
 - Charge stored in cap
- To read
 - Precharge bit and assert wordline
 - Bitline and cap share charge
 - Small change in bitline voltage detected by sense amp
 - Reads are **destructive**
 - Voltage level in the cell degraded after reads
 - Need to refresh (re-write) after each read (done by sense amp)



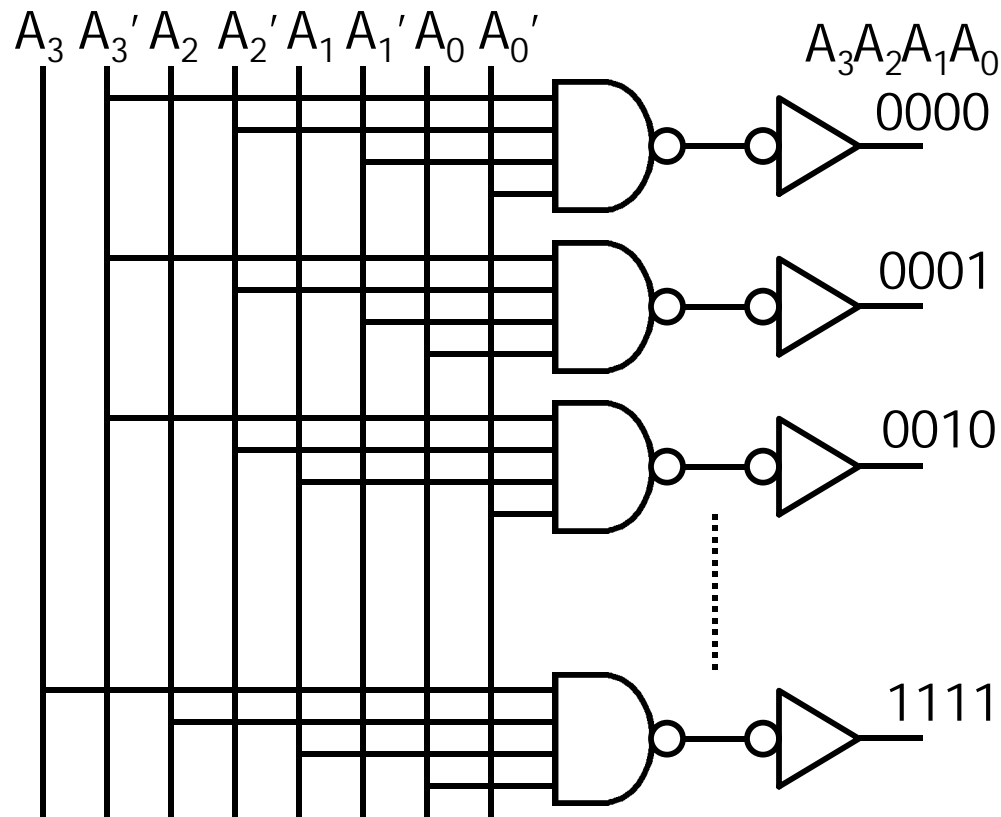
Decoder



- For $n \rightarrow 2^n$ decoder, need 2^n n -input AND's
- Need to be laid out in a regular structure

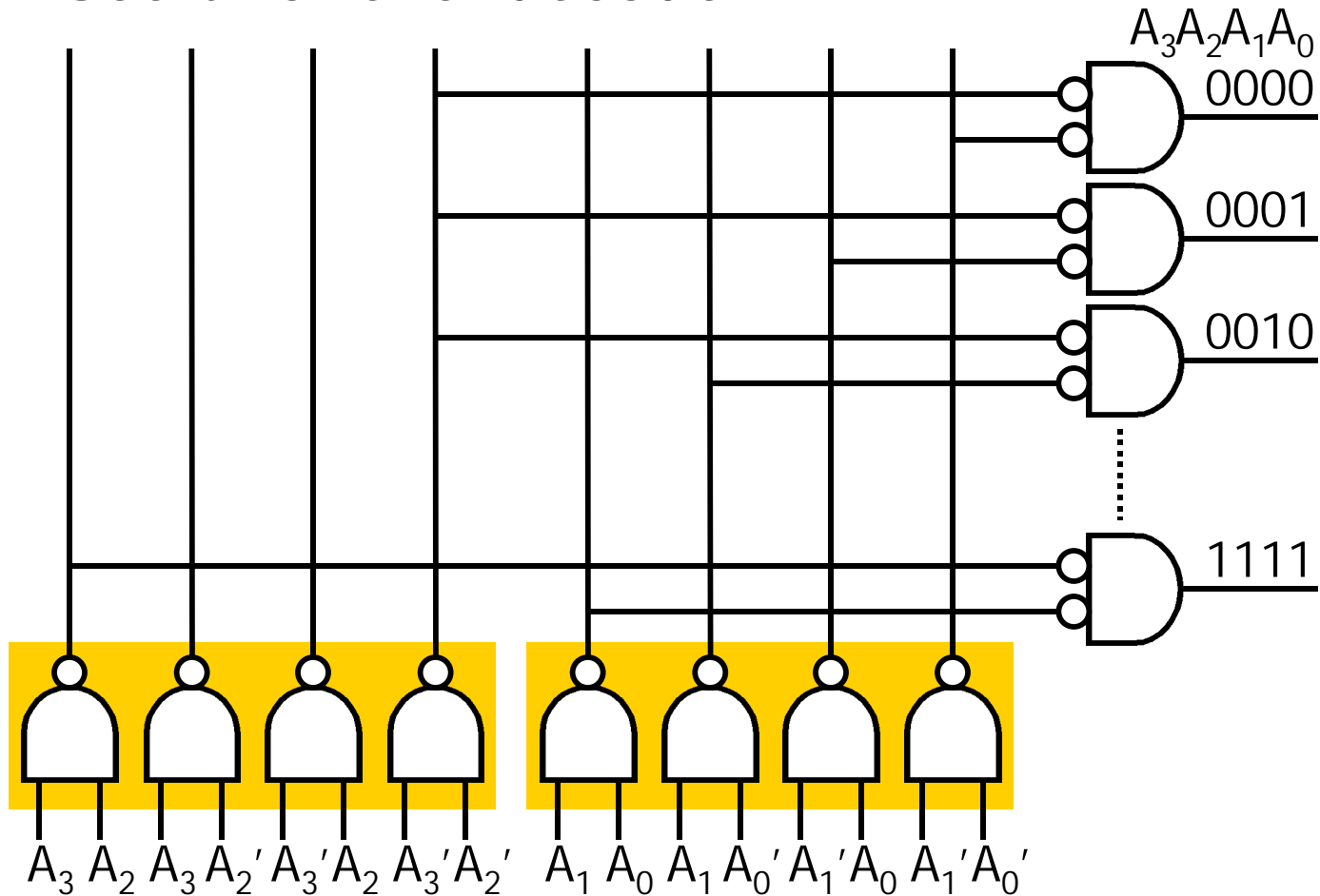
CMOS Decoder

- Large fanin AND gates are problematic



Two-Level Decoder

- Use two-level decoder



With predecode



Predecode

- Predecode binary address into **octal** address
 - For example, 9-bit address ($A_8 A_7 \dots A_0$) can be decoded in two-level
 - Predecode $A_8 A_7 A_6$, $A_5 A_4 A_3$, and $A_2 A_1 A_0$ using 24 3-input NAND's
 - Followed by 512 3-input NOR's

Column Multiplexor

- Given 256 columns, want 32-bit output
- Need 8:1 column muxes
- Build as part of the domino circuit formed by bit cell
- Layer assignment
 - Select lines in poly strapped with M2
 - Bit lines in M1

